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Publisher's version / Version de l'éditeur:
https://doi.org/10.1016/j.orgel.2015.11.039
Organic Electronics: physics, materials, applications, 29, pp. 114-119, 2015-12-14

Inkjet printed thin and uniform dielectrics for capacitors and organic thin film transistors enabled by the coffee ring effect

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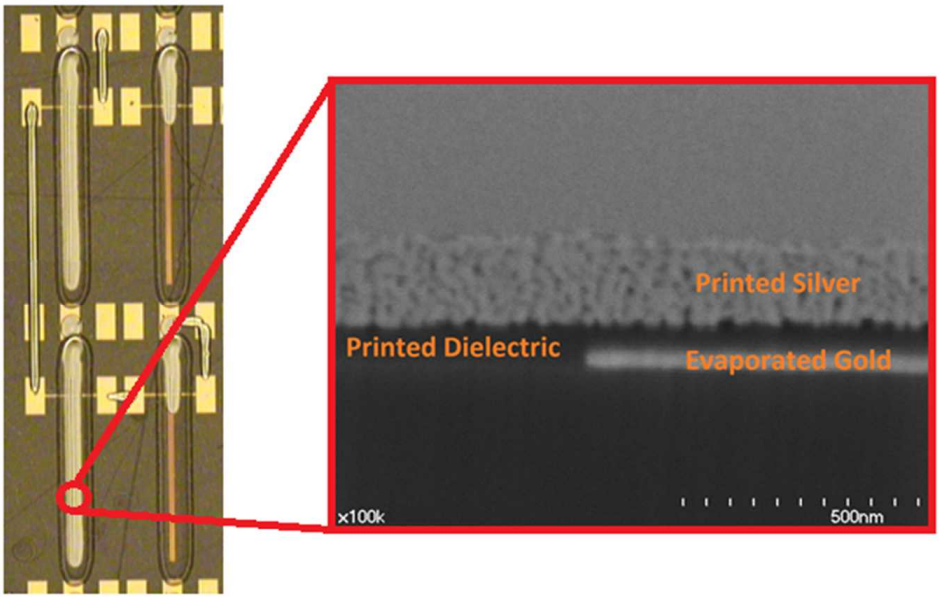
Abstract

The deposition of a thin and uniform dielectric layer is required for high performance printed capacitors and thin film transistors (TFTs), however this is difficult to achieve with printing methods. We have demonstrated inkjet-printed dielectrics with a uniform thickness from 70 nm to 200 nm by taking advantage of the coffee ring effect. A high capacitance per unit area of 230 pF/mm^2 is achieved from capacitors with linear morphologies fully printed onto flexible substrates. We also demonstrate organic TFTs with an average mobility of 0.86 cm^2/Vs and a source drain current of 57 µA obtained with a supply voltage of 15 V. This performance was shown to be consistent, with a standard deviation of 15% obtained from hundreds of printed organic TFTs on PET substrates. This consistency was further validated by the production of functional NAND, NOR, AND and OR logic gates. Our results demonstrate that the coffee ring effect, which is usually viewed as undesirable, can enable higher performance in printed electronic devices.

Graphical Abstract



Highlights

- Printed uniform dielectric layers as thin as 70 nm have been demonstrated.
- This is enabled by taking advantage of the coffee ring effect.
- Printing parameters were optimised to enhance the coffee ring effect.
- Fully printed capacitors with high capacitance (230 pF/mm^2) were achieved.
- The thin and uniform dielectric enabled high performance TFTs and logic gates.

Keywords

Printed electronics, inkjet, polymer dielectric, capacitor, TFT

1. Introduction

The field of printable electronics is one of intense research focus. Printable electronics has the potential to enable low cost, large area and flexible devices to be produced with a myriad of functionalities. Recently reported devices fabricated using printing techniques include photovoltaics [1], organic light emitting diodes [2], radio frequency identification tags [3] and logic circuits [4]. As the number of proposed applications increase, so do the performance requirements for printed components, both in terms of functionality and form.

The use of printing methods for electronic device fabrication results in many challenges. One key challenge that affects many of the aforementioned applications is the printing of a thin, uniform and pinhole-free layer. This is especially crucial for the deposition of and dielectrics for capacitors and transistors. Dielectric layer performance is defined by the relative permittivity (k) of the material, planar area of the layer and the layer thickness. Popular dielectric inks are usually polymer based, such as poly-4-vinylphenol (PVP) [5, 6], polyimide (PI) [7] and poly(methyl methacrylate) (PMMA) [8], all of which are limited to low-k values between 2.6 and 4.3 [9, 10]. This limits the capacitance per unit area, especially in printed applications where very thin dielectric layers are hard to achieve. In order to increase the k value of the dielectric it is common to add high-k materials such as barium titanate ($BaTiO_3$). This approach has been often reported in the literature [6, 11, 12, 13], with k values of printed dielectrics reported as high as 102 [13]. However the approach has limitations [14], chiefly of which is the difficulty in obtaining a thin, defect free film with a suitable nanoparticle loading. Lim *et al.* [12] demonstrated that the k value of a hybrid $BaTiO_3$ inkjet printed film is dependent upon the particle size, with 100 nm diameter particles resulting in a k value of 46, compared to 62 for 500 nm particles. Larger particle sizes will have a significant impact on minimum film thickness and surface roughness. For example, of the aforementioned $BaTiO_3$ articles the reported printed dielectric layer thickness varies between 1.06 µm [6] and 15 µm [12].

Device performance improvements can be made by using thinner dielectric layers using polymer inks. However obtaining a thin and pinhole free film is problematic using printing techniques, with many factors influencing the film quality. These include substrate roughness, drying parameters and environmental conditions. Noh *et al.* [8] demonstrated ultra-thin polymer dielectric layers down to

30 nm by use of a blending PMMA with a crosslinking agent. This was then deposited by spin coating onto glass. Repeating this result onto flexible substrates using high-throughput patterning techniques such as printing will be problematic due to instabilities not present in the spin coating process. Rotary printing methods such as gravure or flexography introduce layer instabilities during the ink splitting phase, while inkjet printing deposits droplets in a discrete fashion, all of which can result in non-uniform layer deposition.

A further problem with solution deposited dielectrics is the 'coffee ring effect', wherein fluid dynamics during the drying process results thicker films at the edges of printed features [15]. This effect is well studied, with the exact morphology of the resulting film dependent upon many variables, including substrate temperature [16, 17], drop spacing [16, 17], humidity [18], solvent vapour pressure [19], drying conditions [20] and ink formulation [21]. It has been shown that this effect can be suppressed by careful solvent selection or optimised printing parameters [16]. Although the coffee ring effect is usually seen as undesirable, useful applications have been demonstrated such as microwells [22], microelectromechanical relays [23] and narrow features [24]. It has been shown that the coffee ring effect can lead to thin and uniform films in the centre of a feature [18, 20]. We propose that the control of this effect in a printed line can lead to thin and reliable films which can be used for printed dielectric applications.

We propose devices which take advantage of the coffee ring effect in order to minimise the dielectric layer thickness. The proposed technique is to control the flow towards the extremities of the feature to leave a thin and uniform valley region in the centre. This effect is easiest to achieve via inkjet printing single droplets or lines, due to the non-contact raster scan method used for printing. As a result devices should be constructed of lines of dielectric, requiring linear morphology capacitors or TFTs. The coffee ring effect needs to be optimised to obtain a wide and thin valley region for maximum capacitance per unit area.

We have realized high performance inkjet printed capacitors and organic TFTs on flexible substrates with ultra-thin dielectric layers. We achieve this by taking advantage of the coffee ring effect in order to achieve a thin and uniform layer in the centre of printed lines. The coffee ring effect was studied with respect to various printing parameters in order to understand the required printing conditions for optimal performance. Inkjet printed dielectric layers with thickness as low as 70 nm have been achieved on printed silver electrodes. We prove the viability of these dielectric layers by producing fully printed capacitors with high capacitance per unit area. In addition, our 3-layer printed organic TFTs achieved an average mobility of 0.86 cm^2/Vs with a relative standard deviation of 15%. This high performance and consistency enabled the production of printed logic gates.

2. Materials and Methods

All printing was performed using a Dimatix 5000 series drop on demand inkjet printer using a nominally 10 pl droplet print head in ambient atmosphere. Printing parameters such as waveform and voltage were optimised for each ink.

For dielectric morphology characterisation prints were made on Si wafers onto which 20 nm of Ag had been thermally evaporated to simulate an ideal printed bottom electrode. The PVP based

dielectric ink was used as purchased from Xerox Research Centre Canada (XRCC). The dielectric constant of 3.9 is obtained when the ink is cured for 10 min at 90 °C followed by 20 min at 130 °C. Morphology was investigated using stylus profilometry (Veeco Dektak 150) and AFM (Veeco EnviroScope). The effects of drop spacing, line width and substrate temperature upon the coffee ring morphology were studied.

Capacitors were printed onto planarised PET substrate (DuPont Melinex ST505). Bottom electrodes were printed using SunJet EMD5603 nanosilver ink which was cured at 130 °C for 20 min. The dielectric layer was then printed using previously optimised settings. Samples were then plasma treated in air at 25 W for 30 s prior to the top electrode deposition using the same parameters as the bottom electrodes. Devices were analysed using a HP 4285A LCR meter, assuming a parallel model.

Transistors were also fabricated on planarised PET. Au source and drain electrodes were fabricated using conventional lift off photolithography. The semiconducting polymer was DPP-Thieno[3,2-b]thiophene copolymer (PDBT-co-TT) [25], purchased from XRCC. This was dissolved in 1,2-dichlorobenzene at a concentration of 5 mg/ml. This was then inkjet printed at a drop spacing of 20 µm using previously optimised print settings. The print was then heated at 90 °C for 10 minutes followed by 140 °C for 20 minutes in a vacuum oven. The dielectric layer was printed using previously optimised settings. Samples were then plasma treated in air at 25 W for 30 s prior to the top electrode deposition using the same parameters as the capacitor electrodes. Devices were analysed using a HP 4155C semiconductor parameter analyser.

3. Results and Discussion

3.1. Dielectric Morphology

The morphology of the printed dielectric is dependent upon a number of printing conditions which include drop spacing, print width and substrate temperature. The effects of these parameters upon the coffee ring morphology are shown in Figures 1 to 3. In particular we examine two parameters of the printed lines, namely the ratio between the valley width and the total width of the printed line and the average height of the valley. The ratio between valley and total width is important as the outer peaks contribute significantly to the planar area whilst being significantly thicker than the centre valley. Therefore it is useful to maximise the valley width with regards to the total width for optimal capacitive structures. The central valley height is the key parameter, as the capacitance is inversely proportional to the dielectric thickness.

Figure 1 shows the effect of drop spacing upon the morphology of a single droplet wide line. Single droplet wide lines were printed with varying drop spacing between 15 and 55 µm. Below 15 µm the centre area thickness was too high to be of interest for this application, above 55 µm the line became irregular. This drop spacing range is larger than expected based on the results of Soltman *et al.*, however there are two significant differences between the tests. In their tests the jetting frequency was much lower, which changes the fluid dynamics during drying as the timescales for the drops to merge are different. Also the fluid properties of their ink are significantly different to the ink used in this study, as is emphasised by the significant coffee ring effect observed in our results.

Increasing the drop spacing results in a narrower line, with a thinner and wider valley section. This is caused by the reduced volume of ink deposited. The minimum measured thickness decreases to a minimum of approximately 60 nm at 55 µm drop spacing. It is also interesting to note that the minimum valley height and maximum peak height appear to be directly proportional and independent of drop spacing, with a constant of proportionality of 0.17 ± 0.01. This is similar in behaviour to the printed Ag ink seen by Kang *et al.* [17] which had a constant value of 0.65 ± 0.05. The lower magnitude seen in our results may be due to the high vapour pressure and lower viscosity of the dielectric ink. This ratio describes the amount of flow from the centre of the printed drop to the edges, and should be minimised to obtain thinner films in the valley region.

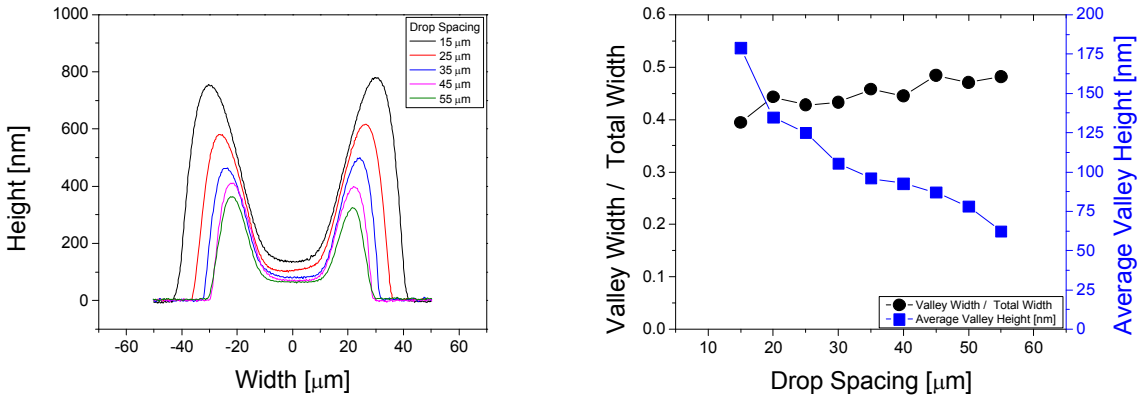


Figure 1. Left: Average line profiles of a single droplet wide line at varying drop spacing. Right: Effect of drop spacing on the ratio between valley width and total width, and the average valley height.

To maximise the planar area of any devices it would be advantageous to widen the valley structure. To achieve this it is possible to print with multiple nozzles in a single pass, as long as the line still forms a uniform coffee ring morphology. It is important to note that printing lines in multiple passes results in a non-uniform layer. Figure 2 shows the morphological results of printing lines with up to three adjacent nozzles. It can be seen that the valley width increases with increasing line width, however the valley height and peak height also increases. This results in an increasing valley to peak height ratio as the width increases. However it can also be seen that the ratio between the valley width and the total width also increases with increasing line width, meaning that the useful proportion of the total width (for maximum capacitance per unit area) is increased.

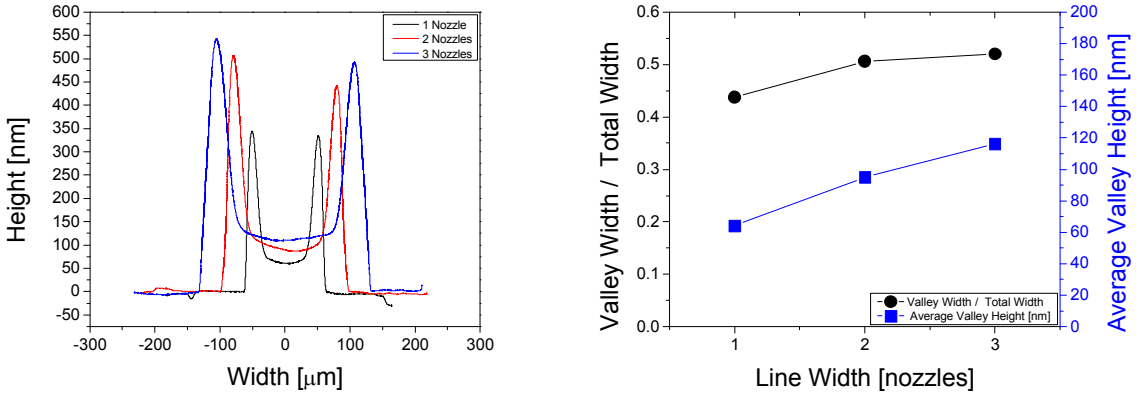


Figure 2. Left: Average line profiles of varying pixel width lines printed with corresponding number of nozzles. Right: Effect of line width on the ratio between valley width and total width, and the average valley height.

The effect of substrate temperature upon the coffee ring morphology was also investigated, as the coffee ring effect is strongly influenced by the drying profile of the ink. Lines were printed at substrate temperatures of 30 °C, 40 °C and 50 °C, with all other printing conditions kept constant. The resulting line profiles are shown in Figure 3. It can be seen that increasing print temperature results in a narrower line with taller peaks and thicker valleys. The narrowing of the lines at higher temperatures is likely due to faster solvent evaporation resulting in less time for the ink to spread on the substrate.

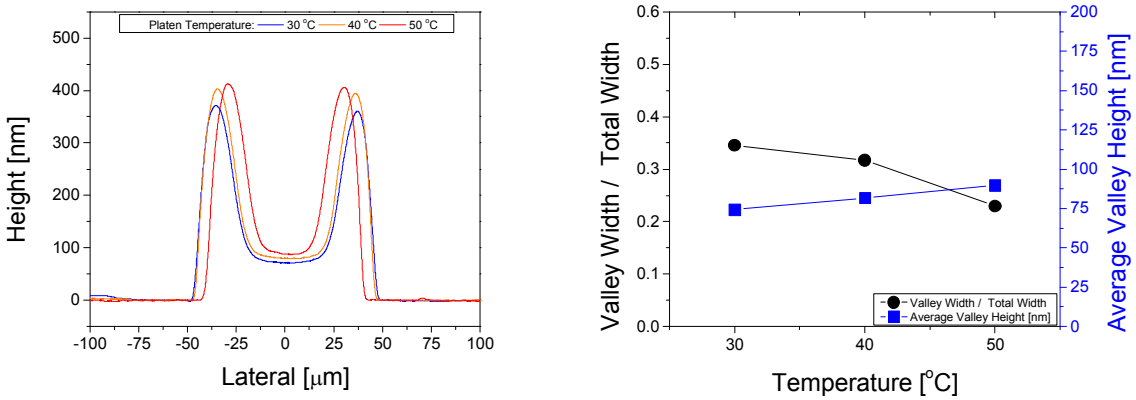


Figure 3. Left: Average line profiles of lines printed at varying platen temperatures. Right: Effect of substrate temperature on the ratio between valley width and total width, and the average valley height.

The roughness of the valley area of the inkjet printed dielectric layer was measured by AFM, which showed an RMS roughness (R_q) of only 0.8 nm, highlighting the uniformity of the surface. This is

essential for printed devices, as non-uniformity of this surface would lead to poor device yield due to shorting.

These morphological characterisation results demonstrate reliable printing of uniform dielectric layers with thicknesses below 100 nm. It has been seen that increased drop spacing, narrower lines and lower substrate temperatures result in thinner films at the centre of the printed features. As previously discussed, this morphology only occurs in single droplets or lines printed in a single printhead pass. Therefore practical devices must be designed such that they are constructed of linear structures, whether this is as isolated single lines or multiple lines connected in parallel. It could also be envisioned that devices such as capacitors could be integrated into interconnect traces in printed circuits. Devices constructed of multiple parallel lines should be optimised to minimize the coffee ring peak width and spacing between adjacent lines in order to maximise the capacitance per unit area.

3.2. Capacitor Devices

We utilised the coffee ring effect to fabricate fully printed capacitors with thin dielectric layers. Figure 4 shows the morphology of a representative device, with the dielectric layer printed at a drop spacing of 25 µm. The key to obtaining reliable fully printed devices is to minimise the roughness of the bottom electrode. The optimised printing conditions gave an R_q at the silver surface of 14 nm**.** This low roughness minimises the risk of shorts through the thin dielectric layer. The capacitor has a minimum dielectric thickness of 70 nm and a mean dielectric thickness of 188 nm. Devices were printed of varying lengths between 10 and 25 mm.

Theoretical device performance was calculated by integration across the dielectric profile shown in Figure 4 within the boundaries of the top electrode; this gave a capacitance per unit area of 255 pF/mm^2. Representative device performance is shown in Figure 5, with a capacitance of 335 pF obtained from an area of 1.45 mm^2, giving a capacitance per unit area of 231 pF/mm^2. The drop in capacitance above 10 kHz is likely due to dielectric polarisation, which is dependent upon material selection. To obtain similar device performance within the same planar area but with a dielectric thickness of 1 µm (a commonly reported thickness for printed dielectrics) a dielectric constant of approximately 26 would be required, for which few printable materials are available.

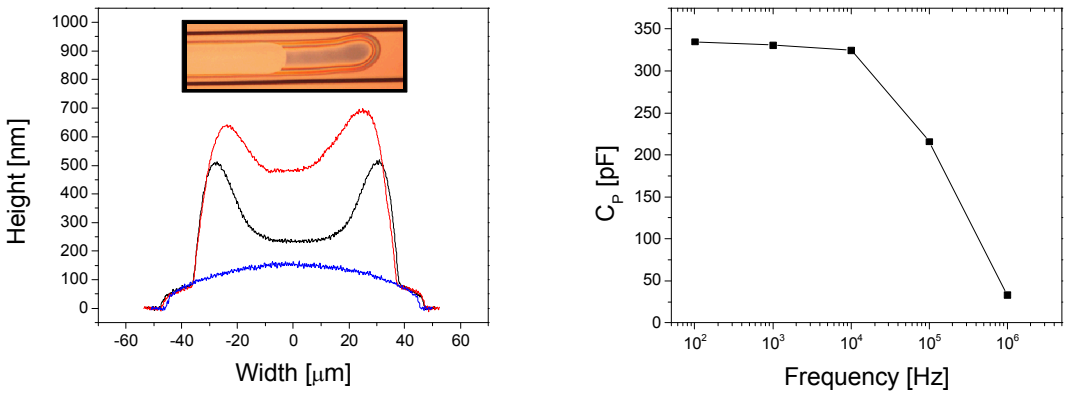


Figure 4. Left: Profile cross section and optical image of fully printed capacitor with a linear morphology. Right: Capacitance as a function of frequency for a linear morphology capacitor of area 1.45 mm^2. This device has a capacitance per unit area of 231 pF/mm^2. Measurement was taken at 50 mV_{RMS}.

3.3 TFT Devices

Thin and uniform dielectric layers are also essential for good performance and uniform production of TFTs and subsequent devices. Top gate architecture devices with parallel source and drain electrodes provide a convenient linear morphology with which to take advantage of the coffee ring effect in the dielectric layer. Three-layer printed devices were produced as described above. Figure 5 shows a cross sectional SEM image of a functional three-layer printed device. The uniformity of the thin printed dielectric layer is clearly visible, with an approximate thickness in the channel area of 90 nm.

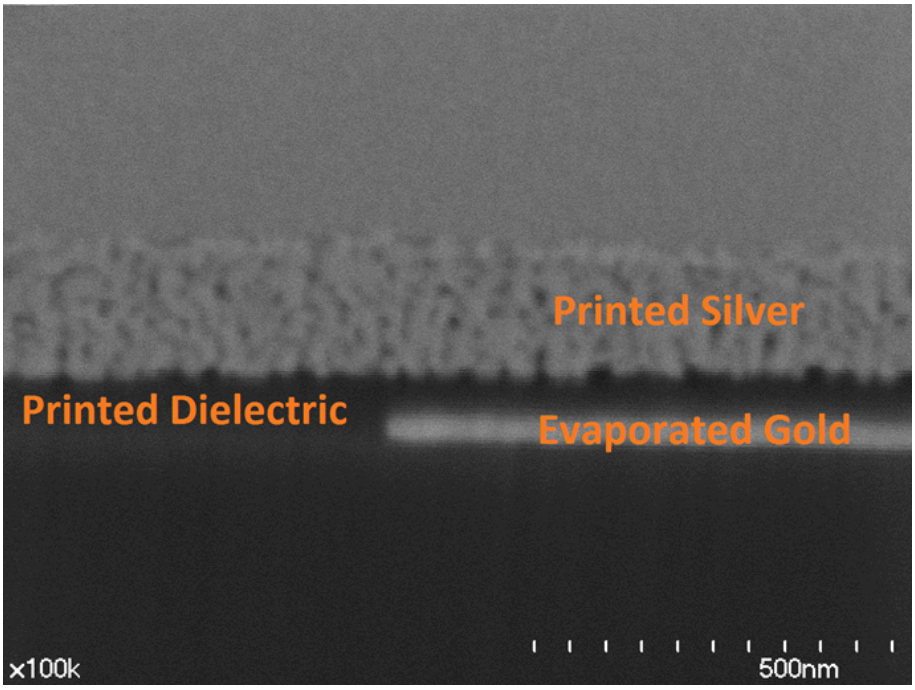


Figure 5. SEM image of a cross section through a three-layer printed TFT. The printed semiconductor layer is not visible.

Representative device performance characteristics are shown in Figure 6. Leakage current is negligible and devices were reliably driven at voltages of 15 V. The devices had a channel length of 5 µm and a channel width of 1 mm, which were defined by the pre-patterned Au electrodes. The thickness of printed semiconductor and dielectric layers are 10 nm and 250 nm, respectively. Although the devices shown in Figure 5 were functional, optimal performance required driving voltages above the breakdown voltage of the dielectric layer. Alternative semiconductor and dielectric materials should enable the exploitation of the thinner layers that we have demonstrated the coffee ring technique is capable of.

Analysis of 220 devices showed an average mobility of 0.86 cm^2/Vs with a relative standard deviation of 15%. Devices with a channel length of 5 µm and a channel width of 1 mm showed an average source-drain current of 57 µA with a relative standard deviation of 15%. This variability is low for printed devices, which highlights the uniformity of the printed dielectric layer. This result can be benchmarked against the results of Y. Li *et al.* [25]. Their devices were manufactured by spin casting PDBT-co-TT on octyltrichlorosilane (OTS) treated SiO_2/Si with an annealing temperature of 140 °C. These devices had a similar dielectric thickness (~200 nm) and the same dielectric constant (3.9) as our printed devices. They reported mobility between 0.5 cm^2/Vs and 0.82 cm^2/Vs with a supplied voltage of 70 V.

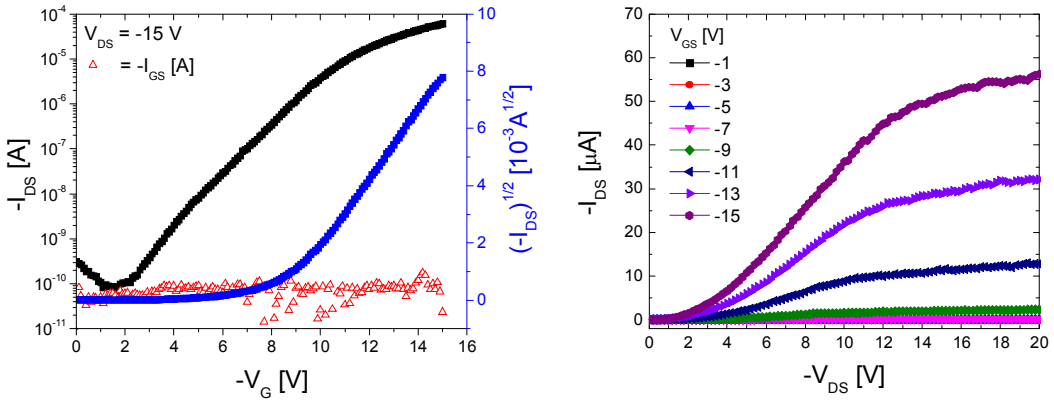


Figure 6. Left: transfer characteristics and measured leakage current of a representative TFT measured at a V_{DS} of -15 V. Right: Output characteristics of the same device.

This excellent printed performance and uniformity of the OTFTs enables the fabrication of more complex circuits, such as logic gates. Figure 7 shows an optical image of a printed NAND gate along with output characteristics of four logic gate types (NAND, AND, NOR, OR).

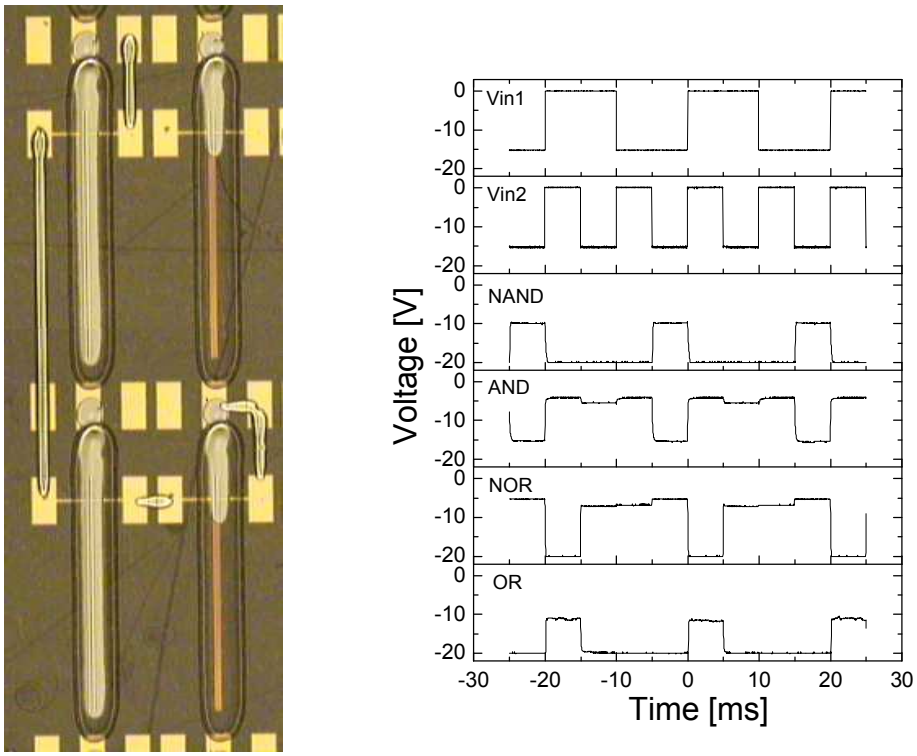


Figure 7. Left: optical microscope image of a printed NAND gate. Right: output characteristics of printed NAND, AND, NOR and OR logic gates. Note that the input voltage is negative.

4. Conclusions

In this study, we have demonstrated a strategy for printing thin and uniform dielectric layers. This strategy combines maximisation of the coffee ring effect to provide a thin and uniform valley area and device designs with linear morphology in order to take advantage of this coffee ring effect. The combination of these techniques enables printable devices with high capacitance per unit area. We have shown dielectric layers as thin as 60 nm with a low R_q of 0.8 nm, which are not normally achievable via printing methods. The practicality of the technique was proven by production of all printed linear morphology capacitors and organic TFTs. The capacitors achieved a capacitance per unit area of over 200 pF/mm^2 despite using a low *k* (3.9) PVP based dielectric. Higher *k* materials would further improve the capacitance per unit area. The uniform and thin dielectric layers also enabled OTFTs with excellent performance, yield and consistency. An average mobility of 0.86 cm^2/Vs and a high average source drain current of 57 µA was achieved in hundreds of OTFTs printed on PET substrate. The uniformity and performance of these devices enables the successful fabrication of various logic gates.

Acknowledgements

The authors would like to acknowledge technical support from Hiroshi Fukutani, Stephen Lang, Eric Estwick, Raluca Movileanu, Richard Dudek, Jeff Fraser and Craig Storey. This work was performed as part of the Printable Electronics program at the National Research Council of Canada.

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