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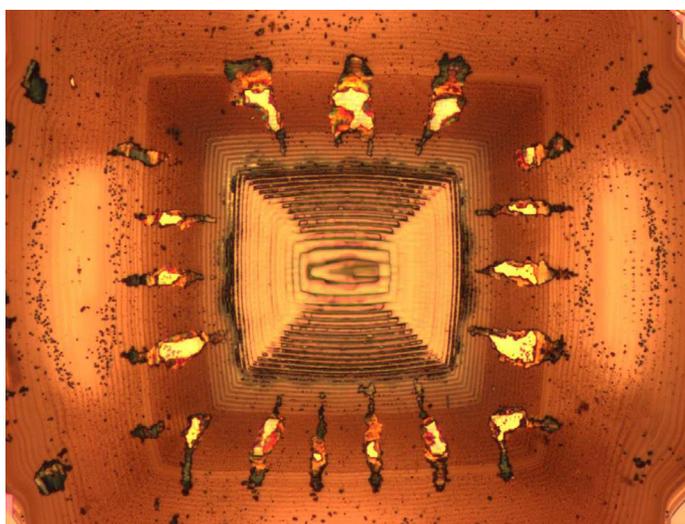
# Uncovered

## Aztec pyramid Electrochemical etching of Te-doped gallium arsenide structures

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Those with vivid imaginations might think that the image on this issue's cover is an aerial view of the Spanish conquistadors, on horseback, preparing to assault the palace of the Aztec leader Montezuma-II in 1520 CE. In reality it is the result of the electrochemical etching (ECE) [1] of a tellurium (Te) doped gallium arsenide (GaAs) molecular beam epitaxy (MBE) structure. Te is an *n*-type dopant in GaAs, and is incorporated on the As sites in the crystal lattice. This dopant can be used controllably to produce

electrical carrier concentrations in the range  $1E16$  to  $>1E19/cm^3$ . The complete structure was a series of five  $\sim 350$  nm thick Te-GaAs layers, in which the Te concentration was decreased stepwise from  $\sim 1E19/cm^3$  near the initial substrate to  $\sim 1E17/cm^3$  at the final growth surface. This was achieved by reducing the temperature of the source of the Te atoms for each layer. By subsequent analysis the temperature of the Te source can then be related to the amount of Te incorporated in each layer. Once this calibration is completed complex structures can then be grown with the accurately controlled carrier concentrations that are necessary for 'state-of-the-art' device performance.

ECE was used, together with capacitance vs. voltage (CV) analysis, to measure the carrier concentration variation of the structure. This was carried out from the surface of the layer, as a function of depth in 10 nm increments, to the underlying substrate. The etching was performed using a WEP CVP21 ECV profiler [2], with a 3 mm diameter sealing ring to define the etched area. The electrolyte used was the traditional ammonium tartrate/ammonia solution [3]. Optical illumination was used during etching to generate electron/hole pairs, and the dissolution current was controlled at  $1 \text{ mA/cm}^2$  ( $\sim 70.7 \mu\text{A}$ ). Using Faraday's laws of electrolysis, the time to remove 10 nm of GaAs was automatically calculated, and the etch process was then stopped to enable a CV measurement to be carried out, and a calculation of the carrier concentration to be made. This was repeated one hundred and seventy five times, until the etch depth was  $\sim 1.75 \mu\text{m}$ , to generate a graphical depth profile of the Te-doping variation.

Normally, if the final epitaxial surface is defect free, the etching proceeds in a planar manner. However, this particular sample had a large number of optically visible defects ( $\sim 700/cm^2$ ), which served as the nucleation sites for the features that were observed at the termination of the ECV measurement sequence. The features are etch pits, with overall dimensions  $\sim 500 \mu\text{m} \times 500 \mu\text{m}$ . That they are pits can be seen in cleaved section, although they can appear to the eye to be raised pyramid-like structures. Since the GaAs substrate had a [1 0 0] crystal surface, the sides of the pyramid are the slow etching {1 1 1} planes of the GaAs cubic crystal lattice, aligned to the two mutually perpendicular (1 1 0) directions.

The formation of pits during etching is due to the presence of crystalline defects, such as dislocations and/or stacking

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faults. Strain fields associated with the defective crystal lattice accelerate the etch process relative to the initial planar surface. In the case of ECE, the strain fields act as low resistance current paths, which result in enhanced material removal. However it is not clear as to why these particular pits formed with the wire-like features regularly arranged around the central inverted stepped pyramid.

Profiles at other locations on the wafer produced the same features. So it is a reproducible, but inexplicable, phenomenon. However, etching using an alternative electrolyte was more planar, but did not produce similar features. So it would appear that these pits are a peculiarity of the ammonium tartrate/ammonia electrolyte ECE process.

#### Further reading

- [1] T. Ambridge, M.M. Faktor, *J. Appl. Electrochem.* 5 (1975) 319–328.
- [2] <http://wepcontrol.com/cv-profiler/index.htm>.
- [3] PN 4200 Polaron's Semiconductor profiler, Instruction manual, Bio-Rad, Richmond, CA.



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