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PREPARED BY SLee	OTTAWA, CANADA	COPY NO. 13
CHECKED BY PYKim	LABORATORY MEMORANDUM	DATE October 1981
	SECTION ENGINE LABORATORY	

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SUBJECT TRACKING OSCILLATOR WITH ADJUSTABLE OFFSET

PREPARED BY S. LEE*

*Summer Student
3rd Year, Massachusetts Institute of Technology

ISSUED TO

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MECHANICAL ENGINEERING
LABORATORY MEMORANDUM

NO. NRC-ENG-114

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MECHANICAL ENGINEERING
LABORATORY MEMORANDUM

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1. INTRODUCTION

The device presented herein is an oscillator which outputs a square wave proportional in frequency to the input to the oscillator. That is, if the input is F_1 and the output is F_0 , the relationship between the two is given by:

$$F_0 = F_1 * K \quad \text{Where } 0.95 < K < 1.05$$

The oscillator is meant to be used with an optical pickup and a stroboscope to view high speed rotors. (See Fig. 1)

If K is set to 1, the rotor appears to be stationary. If K is less than 1, the rotor will appear to slowly rotate in the actual direction of rotation. If K is greater than 1, it will appear to be the opposite.

2. THE CIRCUIT

As shown in the block diagram (Fig. 2), the circuit has 3 major blocks: the input buffer; the frequency synthesis section; and an output buffer.

The input buffer is meant to protect the frequency synthesis section and to provide gain when necessary (minimum gain is unity). The input buffer has two parts, a relay and an amplifier. The purpose of the relay is to prevent any signals from reaching the amplifier when the power is off, and thereby prevent damage. This is necessary as an operational amplifier was chosen for its high input impedance. The amplifier itself is a differential input, single-ended output operational amplifier (one of four on one chip), in a non-inverting configuration. This gives gain from unity upwards, and an extremely high input impedance, greater than 1 megaohm.

The frequency synthesis section has three parts: a frequency to voltage converter, a precision gain amplifier and a voltage controlled oscillator. The operation of this block is as follows: the frequency to voltage converter outputs a voltage from 0 to 12 volts in proportion to an input frequency from 0 to 595 hertz; the precision gain amplifier then amplifies this voltage with a gain between 0.95 and 1.05; the voltage controlled oscillator (VCO) takes this voltage from 0 to 12 volts and outputs a frequency in proportion from 0 to 595 hertz. Thus this block will track a given input and output a frequency whose proportionality is given by the gain of the amplifier. The frequency to voltage converter is implemented using a Motorola 4046B phase-locked loop. This chip has two phase comparators and a voltage controlled oscillator. Phase comparator 1 is simply an EXOR gate. It is very immune to input noise but has the disadvantages of locking on harmonics of the input, and giving an output which has a phase angle with respect to the input. Phase

LABORATORY MEMORANDUM

comparator 2 is a more complex digital network which does not lock on harmonics and gives outputs with no phase lag, but is sensitive to noise. Since a clean input signal was expected, phase comparator 2 and the VCO in the chip were utilized to implement the frequency to voltage converter. (See Fig. 3)

The phase comparator outputs a voltage which is proportional to the difference between input signal and input comparator. This signal is fed into a VCO which outputs a frequency proportional to this signal. The result is then fed back into the comparator and compared again with the input signal to check for any difference. Thus, the comparator adjusts the voltage into the VCO until there is no difference between the VCO output and the signal. This voltage is therefore proportional to the input frequency and is the output of the frequency to voltage converter. At this point another signal, which drives a meter to indicate whether the oscillator is tracking or not, is developed. The chip has an output called Phase Pulse Output. Its output is a square wave whose duty cycle is proportional to the phase difference between the two inputs to phase comparator 2. When the difference is 0 degrees, the duty cycle is 100% (always high). As the phase difference decreases, the duty cycle decreases. The output from this pin is fed to a 741 op-amp in voltage-follower configuration. This is then fed to a meter. When the Phase Pulse Output is high, the meter reads full scale. As the duty cycle decreases, the meter reading decreases, indicating a loss of lock.

The precision gain amplifier is actually two inverting amplifiers hooked in series. One is used to do the precision amplification, and the other is used to ensure that when the gain of the precision amplifier is set to 1, the input and output frequencies match. This is necessary because the VCO does not necessarily have the same proportionality between voltage and frequency that the frequency to voltage converter has. The precision amplifier is set up as shown in Fig. 4. Specific values assigned to the components shown in Fig. 4 are as below.

R1 is adjusted to 10.0 kilohms.

R2 is adjusted to 9.50 kilohms.

R3 is varied from 0 to 1.00 kilohms.

Gain = $K = (R2 + R3)/R1$

Therefore the gain varies from 0.95 to 1.05.

The voltage controlled oscillator block is simply the VCO section of another 4046.

The output buffer is similar to the input buffer, and consists of a non-inverting amplifier and a relay. The amplifier is used to provide gain when necessary, and to avoid loading the output of the frequency synthesis section. The relay is to protect the amplifier outputs when power is disconnected.

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3. CONCLUSION

A tracking oscillator with adjustable offset has been designed for motion analysis.

The circuit exhibits some instability due to the abnormally low frequencies at which the 4046 chips are used (they are meant to operate at about 1 megahertz), and can go out of lock and not be brought back. In that case the power should be turned off then turned back on.

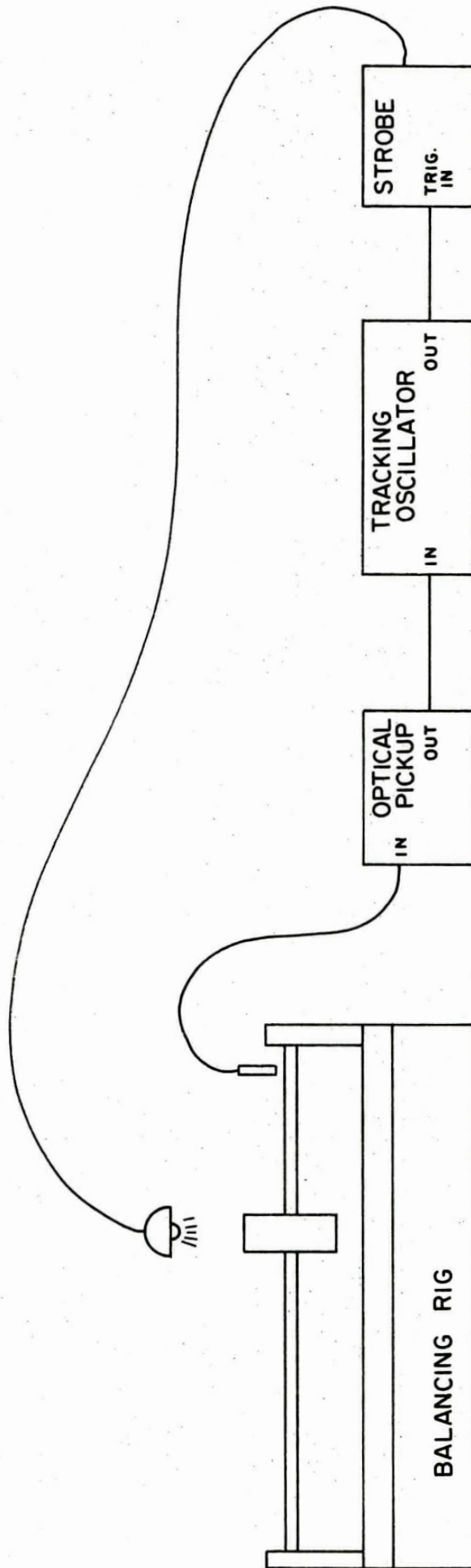


FIG. 1

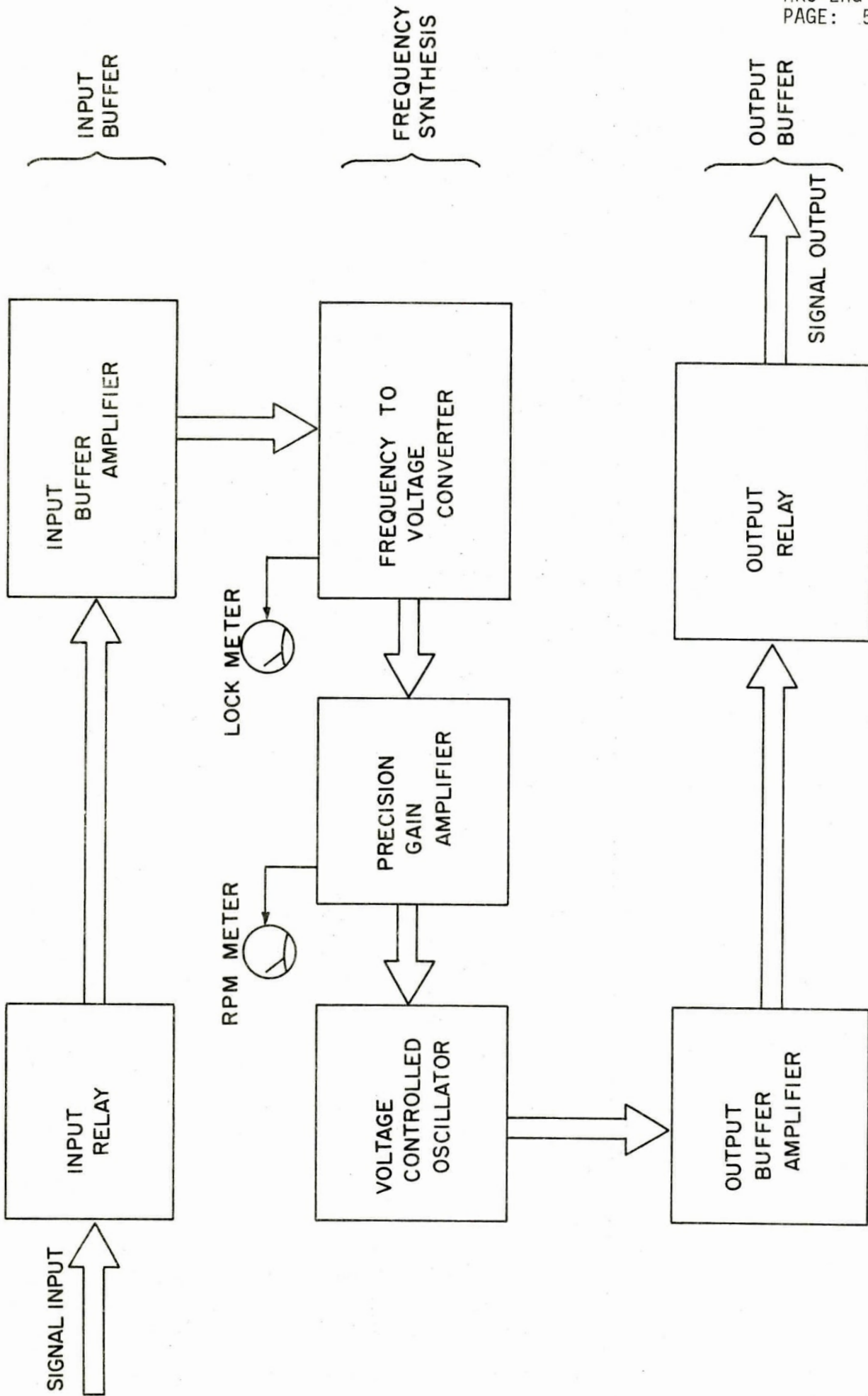


FIG. 2 BLOCK DIAGRAM

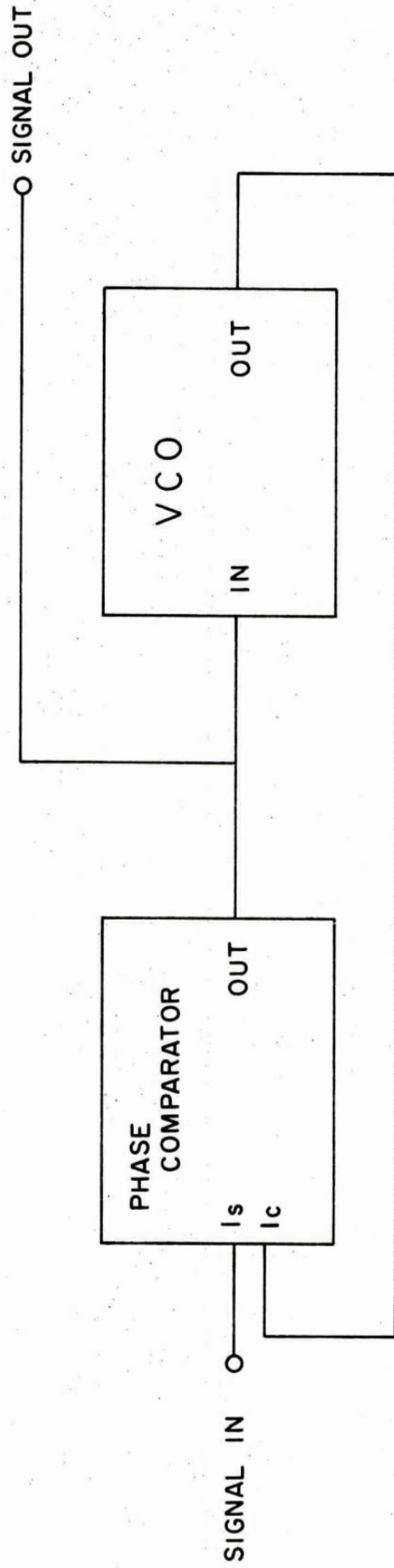


FIG. 3

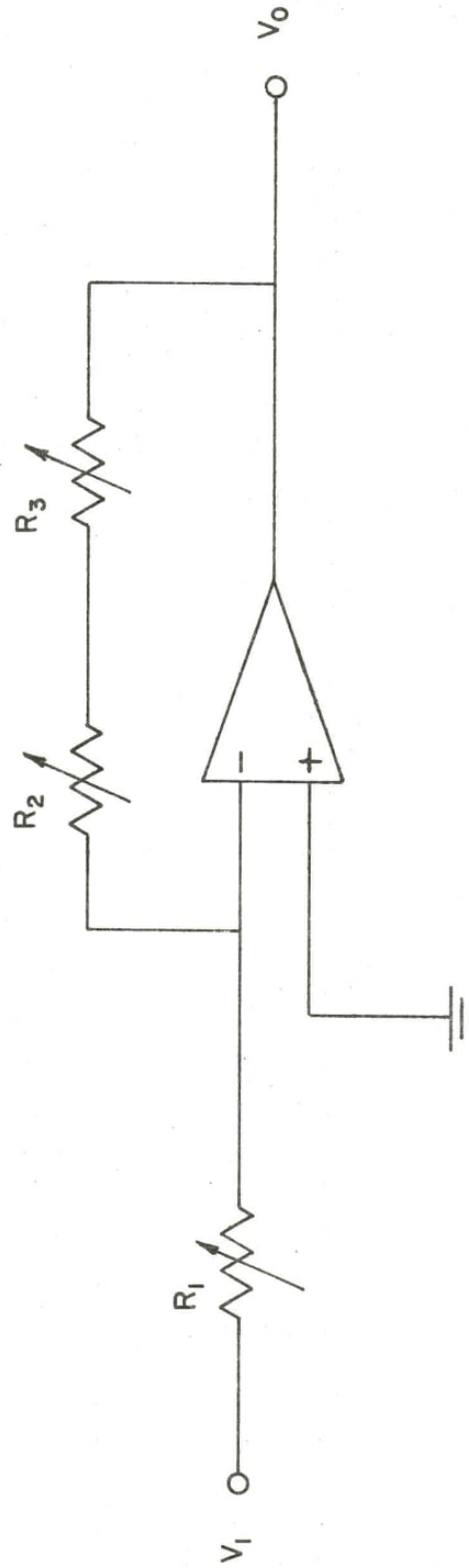
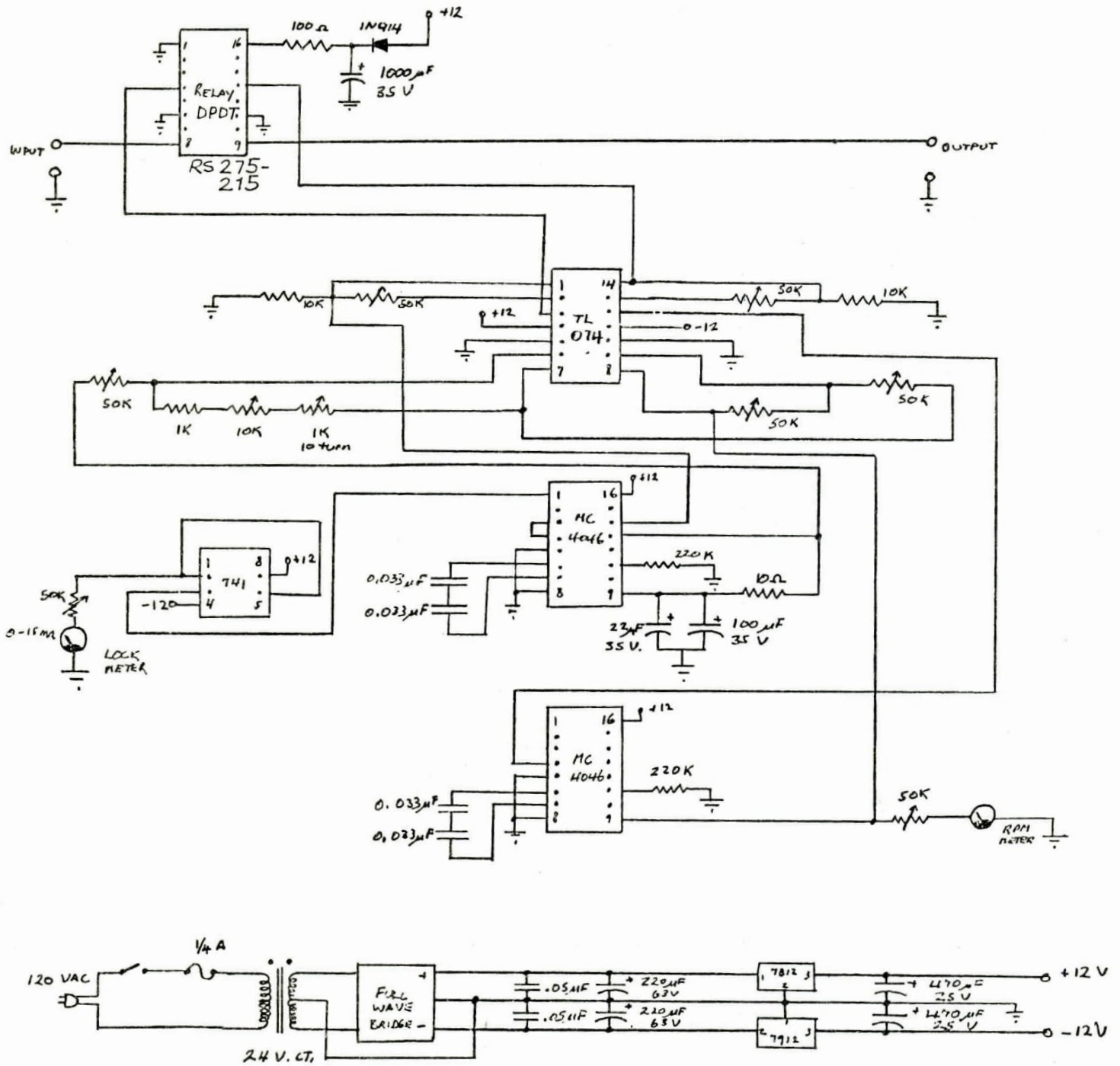


FIG. 4

APPENDIX: CIRCUIT DIAGRAM
AND MISCELLANEOUS INFORMATION
OF PARTS USED

CIRCUIT DIAGRAM



4046B

MICROPOWER PHASE-LOCKED LOOP

DESCRIPTION — The 4046B is a Micropower Phase-Locked Loop consisting of a low power linear Voltage-Controlled Oscillator, a Source Follower Circuit, two different Phase Comparators, and a Zener diode. The Voltage-Controlled Oscillator has two External Capacitor connections (C_{exta} , C_{extb}), two External Resistor connections (R_{exta} , R_{extb}), a Voltage-Controlled Oscillator Input (I_{VCO}) and a Voltage-Controlled Oscillator Output (O_{VCO}). The Source Follower Circuit provides a Demodulated Output (O_D) from the Voltage-Controlled Oscillator. An active LOW Enable Input (\bar{E}) common to both the Voltage-Controlled Oscillator and the Source Follower Circuit is also provided. Phase Comparator I and Phase Comparator II have common Signal (I_S) and Comparator (I_C) Inputs and separate outputs; Phase Comparator I Output (O_{PC1}), Phase Comparator II Output (O_{PCII}), and Phase Pulse Output (O_{P11}). An input to the Zener diode (I_Z) is also provided.

The Voltage-Controlled Oscillator requires one external capacitor (C_1) and one external resistor (R_1) to determine operational frequency range. A second external resistor (R_2) may be used to allow frequency offset. External resistor R_3 and external capacitor C_2 combined serve as a low pass filter to the Voltage-Controlled Oscillator Input (I_{VCO}). Output O_D is provided to avoid loading the low pass filter. External resistor R_4 is required if this output is utilized. O_D must be left open when not utilized. The output from the Voltage-Controlled Oscillator (O_{VCO}) may be connected directly or indirectly through CMOS frequency dividers (i.e., the 4018B, 4020B, 4022B, 4024B, 4029B, 4040B, 4518B, 4520B, 40160B, 40161B, 40162B, 40163B, 40192B or 40193B) to the Comparator Input (I_C). With the Enable Input (\bar{E}) HIGH both the Voltage-Controlled Oscillator and the Source Follower Circuit are OFF to minimize power consumption. With \bar{E} LOW, both are enabled.

For direct-coupling between O_{VCO} and I_C , the voltage swing at the Voltage Controlled Oscillator Output (O_{VCO}) must be within standard CMOS logic levels ($V_{OH} > 0.7 \times V_{DD}$ and $V_{OL} < 0.3 \times V_{DD}$); otherwise the signal from O_{VCO} must be capacitively coupled to the Signal Input (I_S).

Phase Comparator I is an Exclusive OR circuit ($I_C \oplus I_S$). I_C and I_S must have 50% duty cycles to maximize lock range. When the Output of Phase Comparator I (O_{PC1}) is connected back to the Voltage-Controlled Oscillator through the low pass filter network, an averaged voltage to I_{VCO} forces oscillation at a center frequency.

Phase Comparator II is an edge-triggered digital memory network with four flip-flop stages, associated control circuitry and a 3-state output. Phase Comparator II triggers on LCW-to-HIGH transitions at the Signal (I_S) and Comparator (I_C) Inputs and is independent of duty cycle at these inputs. The Output of Phase Comparator II (O_{PCII}) provides voltage levels and duty cycles corresponding to frequency and phase differentials between I_C and I_S . When O_{PCII} is connected to the Voltage-Controlled Oscillator Input (I_{VCO}) through the low pass filter network, a corresponding voltage across capacitor C_2 is adjusted until the Signal (I_S) and Comparator (I_C) Inputs are equal in both frequency and phase. At this point Phase Comparator II maintains a constant voltage across Capacitor C_2 . When this stability has been established, the Phase Pulse Output (O_{P11}) is HIGH indicating a locked condition. Power dissipation in the low pass filter is reduced when Phase Comparator II is used.

A zener diode is provided for regulating the power supply voltage, if necessary.

- VERY LOW POWER CONSUMPTION
- HIGH VCO LINEARITY, 1% TYPICAL
- CHOICE OF 2-PHASE COMPARATORS
- ENABLE INPUT (ACTIVE LOW) FOR LOW POWER DISSIPATION IN STANDBY MODE
- ON-CHIP ZENER DIODE FOR SUPPLY REGULATION
- VCO FREQUENCY DRIFT WITH TEMPERATURE = 0.04% / °C TYPICAL AT $V_{DD} = 10$ V

PIN NAMES

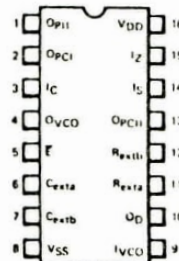
I_Z	Zener Diode Input
I_S	Signal Input
I_C	Comparator Input
I_{VCO}	Voltage-Controlled Oscillator Input
\bar{E}	Enable Input (Active LOW)
C_{exta} , C_{extb}	External Capacitor Connections
R_{exta} , R_{extb}	External Resistor Connections
O_{PC1}	Phase Comparator I Output
O_{PCII}	Phase Comparator II Output
O_{P11}	Phase Pulse Output
O_D	Demodulator Output
O_{VCO}	Voltage-Controlled Oscillator Output

LOGIC SYMBOL



V_{DD} = Pin 16
 V_{SS} = Pin 8

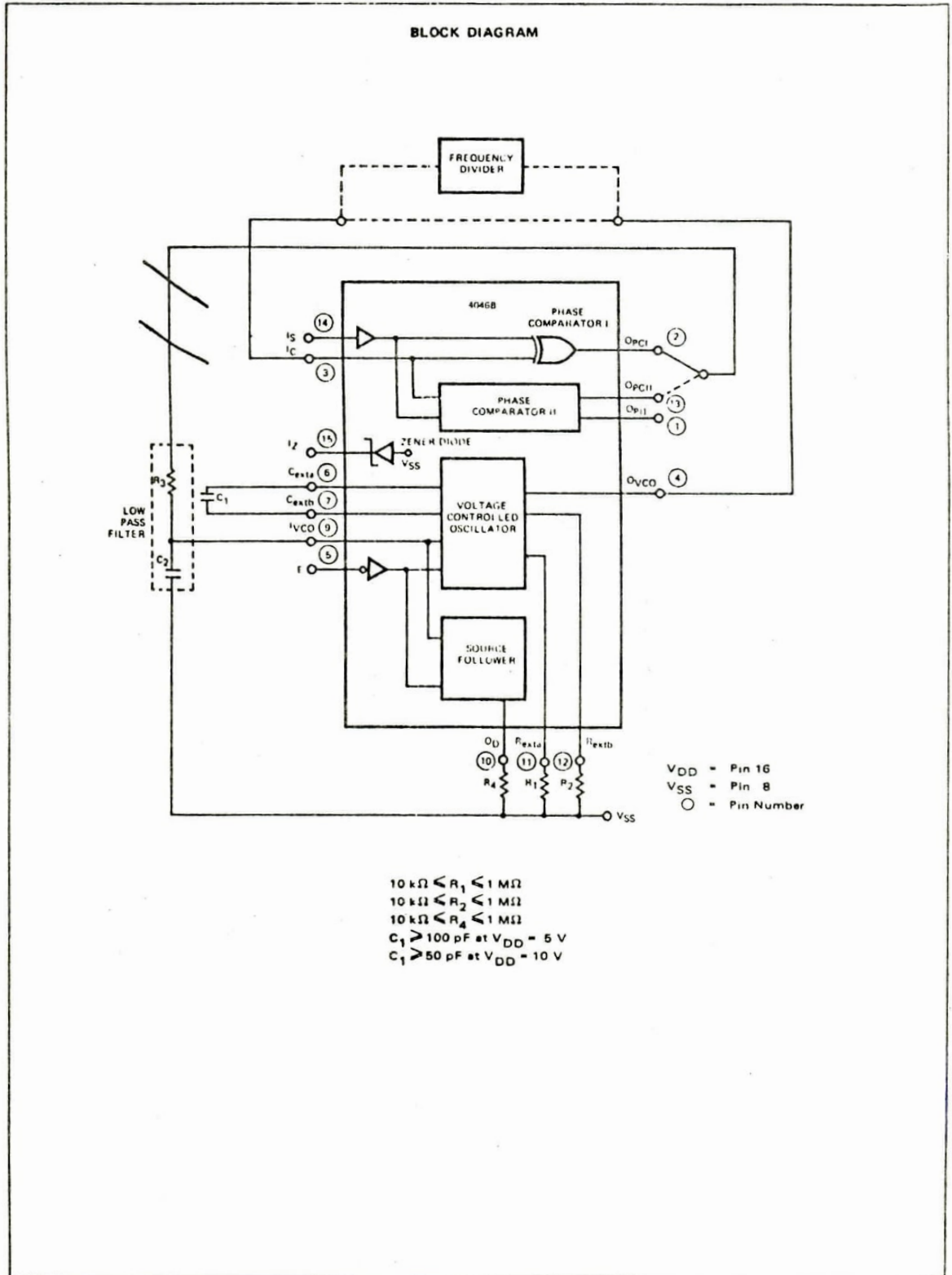
**CONNECTION DIAGRAM
DIP (TOP VIEW)**



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In Line Package.

FAIRCHILD CMOS • 4046B

BLOCK DIAGRAM



$10\text{ k}\Omega \leq R_1 \leq 1\text{ M}\Omega$
 $10\text{ k}\Omega \leq R_2 \leq 1\text{ M}\Omega$
 $10\text{ k}\Omega \leq R_4 \leq 1\text{ M}\Omega$
 $C_1 \geq 100\text{ pF}$ at $V_{DD} = 5\text{ V}$
 $C_1 \geq 50\text{ pF}$ at $V_{DD} = 10\text{ V}$

FAIRCHILD CMOS • 4046B

FUNCTIONAL DESCRIPTION — The 4046B, Micropower Phase-Locked Loop consists of a low power linear Voltage-Controlled Oscillator (VCO), a Source Follower circuit (SF), two Phase Comparators (PC I and PC II) and a Zener diode.

VOLTAGE-CONTROLLED OSCILLATOR

The VCO requires one external capacitor (C_1) and one external resistor (R_1) to determine operational frequency range. External resistor R_2 is used to allow for frequency offset, if required. It is recommended that R_1 and R_2 have a value between 10 k Ω and 1 M Ω . At $V_{DD} = 5$ V, C_1 should be greater than or equal to 100 pF, and at $V_{DD} = 10$ V, C_1 should be greater than or equal to 50 pF.

External resistor R_3 and external capacitor C_2 combined serve as a low-pass filter to the Voltage-Controlled Oscillator Input (I_{VCO}). The user is allowed a wide range of resistor-to-capacitor ratios for R_3 and C_2 because of the high input impedance at I_{VCO} (approximately 10^{12} Ω).

To avoid loading of the low-pass filter, the Demodulator Output (O_D) should be connected through external resistor R_4 as shown in the Block Diagram. It is recommended that R_4 have a value between 10 k Ω and 1 M Ω . If the O_D output is not utilized it must be left open.

The Voltage-Controlled Oscillator Output (O_{VCO}) provides a 0.3 V_{DD} to 0.7 V_{DD} output voltage swing and may be connected to the Comparator Input (I_C). O_{VCO} may also be connected indirectly to I_C via CMOS frequency dividers (i.e., the 4018B, 4022B, 4029B, 4040B, 4518B, 4520B, 40160B, 40161B, 40162B, 40163B, 40192B, and 40193B).

An Enable Input (\bar{E}) to the VCO and SF is provided for minimum stand-by power dissipation. With the \bar{E} Input HIGH both the VCO and the SF are OFF. With \bar{E} LOW, both are enabled.

PHASE COMPARATORS

For direct-coupling between O_{VCO} and I_C , the voltage swing at O_{VCO} must be within standard CMOS logic levels ($V_{OH} > 0.7 V_{DD}$ and $V_{OL} < 0.3 V_{DD}$); otherwise the signal from O_{VCO} must be capacitively coupled to the self-biasing amplifier at the I_S Input.

Phase Comparator I is an Exclusive OR circuit ($I_C \oplus I_S$). For maximum lock range, inputs to I_C and I_S must have 50% duty cycles. (Lock range, $2f_L$, is defined as that frequency range of input signals upon which the 4046B will stay locked from an initial locked condition). With no signal or noise input, Phase Comparator I provides an average output voltage equal to $V_{DD}/2$ at the $O_{PC I}$ Output. This average output voltage is supplied to the I_{VCO} Input through the low-pass filter, which in turn forces the VCO to oscillate at a center frequency (f_0).

Capture range $2f_C$, is defined as that frequency range of input signals upon which the 4046B will lock from an initial unlocked condition. Capture range for PCI is directly dependent upon the characteristics of the low-pass filter network and may be as great as the lock range. Thus, PCI allows the user a phase-locked loop system which will remain in a locked condition despite high amounts of noise in the input signal.

It should be noted that with the use of PCI the system may lock onto input signals with frequencies that are near harmonics to the center frequency of the VCO. It should further be noted that the phase angle between the I_C and I_S Inputs will vary between 0° and 180° . At the center frequency the phase angle is 90° . Figure 2 illustrates a typical Phase Angle versus Average Output Voltage response characteristic for PCI. Figure 3 illustrates the typical waveforms for a phase-locked loop system employing PCI and locked at a center frequency.

Phase Comparator II is edge-triggered digital memory network with four flip-flop stages, associated control circuitry and a 3-state output, controlled internally. PCII triggers on LOW-to-HIGH transitions at the Signal (I_S) and Comparator (I_C) Inputs and is independent of duty cycle at these inputs. If the input frequency at I_S is higher than the input frequency at I_C , the p-channel output transistor at $O_{PC II}$ is turned "ON" continuously, pulling the output ($O_{PC II}$) toward V_{DD} . If the input frequency at I_C is higher than the input frequency at I_S , the n-channel output transistor at $O_{PC II}$ is turned "ON" continuously, pulling the output toward V_{SS} . If the input frequencies at I_S and I_C are equal, but I_S lags I_C in phase, the n-channel output transistor is turned "ON" for a period of time corresponding to the phase difference. If the input frequencies at I_S and I_C are equal, but I_C lags I_S in phase, the p-channel output transistor is turned "ON" for a period of time corresponding to the phase difference. Thus, over a period of time the voltage at capacitor C_2 is adjusted until the I_C and I_S input signals are of the same frequency and phase. Once this stability is reached, both p- and n-channel output transistors at $O_{PC II}$ are "OFF". $O_{PC II}$ becomes an open circuit holding the voltage across C_2 constant.

Once this stability is attained, the Phase Pulse Output ($O_{P II}$) is HIGH indicating a locked condition.

With PCII no phase difference is present between I_C and I_S over the entire VCO frequency range. Furthermore, since the 3-state Phase Comparator II Output ($O_{PC II}$) is mostly in the "OFF" condition, power dissipation through the low-pass filter is minimized. It should also be noted that $2f_C = 2f_L$ independent of the filter network in a phase-locked loop utilizing PCII. Figure 4 shows typical waveforms for a phase-locked loop system employing Phase Comparator II and locked at a center frequency.

FAIRCHILD CMOS • 4046B

Fig. 2 CHARACTERISTICS OF PHASE COMPARATOR I AT THE LOW PASS FILTER OUTPUT.

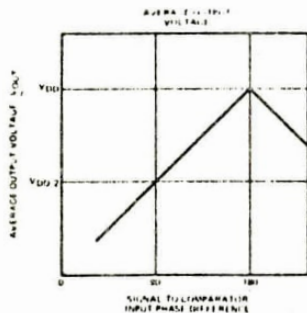


Fig. 3 A PLL SYSTEM USING PHASE COMPARATOR I.

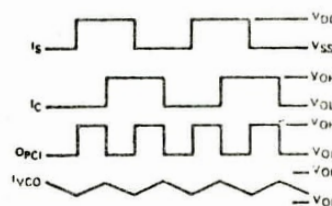


Fig. 4 A PLL SYSTEM USING PHASE COMPARATOR II

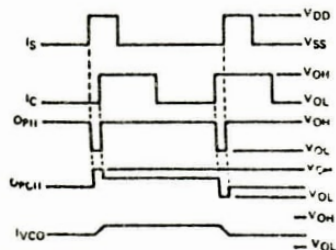


Fig. 5 TYPICAL LOW-PASS FILTERS.

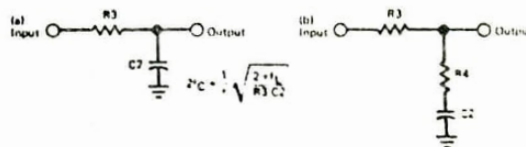
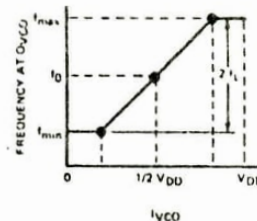


Fig. 6 DESIGN INFORMATION.

Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on Input I _S	VCO in PLL system adjusts to center frequency (f ₀).	VCO in PLL system adjusts to minimum frequency (f _{min}).
Phase angle between I _S and I _C	90° at center frequency (f ₀), approaching 0° and 180° at ends of lock range (2f _L).	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	HIGH	LOW
Lock frequency range (2f _L).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock. 2f _L = full VCO frequency range = f _{max} - f _{min} .	
Capture frequency range (2f _C).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (Figure 5) f _C < f _L	f _C = f _L
Center frequency (f ₀).	The frequency of O _{VCO} when IvCO = 1/2 V _{DD}	
O _{VCO} frequency (f).	$f \approx \frac{K \left[\frac{I_{VCO} - 1.65}{R_1} + \frac{V_{DD} - 1.35}{R_2} \right]}{(C_1 + 32)(V_{DD} + 1.6)} \text{ MHz (at 25°C)}$	
NOTE: The information presented here is meant only as a design guide.	<p>where:</p> <ul style="list-style-type: none"> V_{DD} in V; 5 V < V_{DD} < 15 V I_{VCO} in V; 1.65 V < I_{VCO} < (V_{DD} - 1.35 V) R₁ and R₂ in MΩ; R₁, R₂ > 0.005 MΩ C₁ in pF; C₁ > 50 pF K = 0.95 @ V_{DD} = 5 V = 0.95 @ V_{DD} = 10 V = 1.08 @ V_{DD} = 15 V 	



See last page of data sheet for ordering information.

MC1741, MC1741C MC1741N, MC1741NC

INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Low Noise Selections Offered - N Suffix

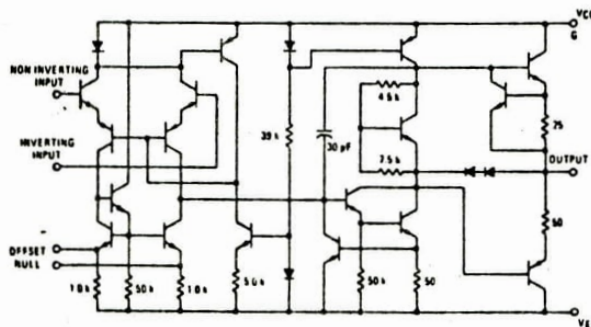
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1741C	MC1741	Unit
Power Supply Voltage	V _{CC}	+18	+22	Vdc
	V _{EE}	-18	-22	Vdc
Input Differential Voltage	V _{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V _{ICM}	±15		Volts
Output Short Circuit Duration (Note 2)	t _S	Continuous		
Operating Ambient Temperature Range	T _A	0 to +70	-55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150		°C
		55 to +125		
Junction Temperature Range	T _J	175		°C
		150		

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

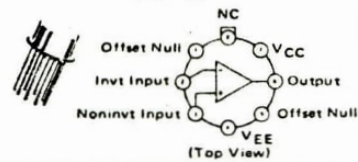
Note 2. Supply voltage equal to or less than 15 V

EQUIVALENT CIRCUIT SCHEMATIC

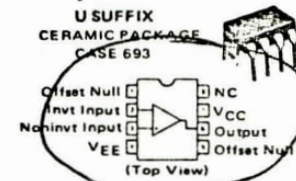


OPERATIONAL AMPLIFIER SILICON MONOLITHIC INTEGRATED CIRCUIT

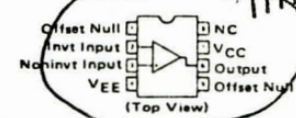
G SUFFIX METAL PACKAGE CASE 601



P1 SUFFIX PLASTIC PACKAGE CASE 626 (MC1741C, MC1741NC)

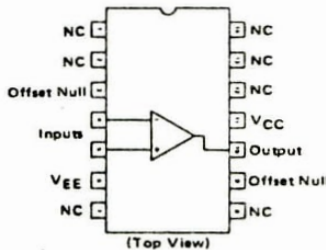


U SUFFIX CERAMIC PACKAGE CASE 693

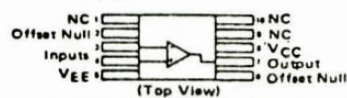


L SUFFIX CERAMIC PACKAGE CASE 632 TO-116

P2 SUFFIX PLASTIC PACKAGE CASE 646 (MC1741C, MC1741NC)



F SUFFIX CERAMIC PACKAGE CASE 606-04 TO-91



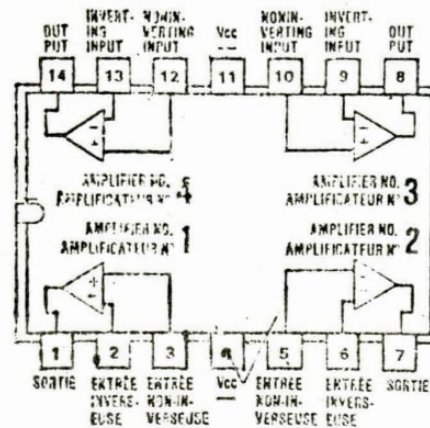
RS 276-1714 OP Amp

RS
276-1714

Features:

- Internally compensated -- Low noise
 - Very high input impedance (>10¹⁰ ohms)
 - Output short circuit protection
 - Suitable for dual ended power supply applications
- Absolute maximum ratings:**
 Supply voltage: V_{CC} = 0V to +15VDC
 Differential input voltage: 15VDC
 Input current: 10mA
 Power dissipation: 600 mW
 Operating temperature: 0°C to 70°C

FOR FURTHER INFORMATION SEE
RADIO SHACK DATA BOOKS



Amplif. opérationnel quadruple à EI-FET de type TL084C

Caractéristiques:

- Compensation interne • Faible niveau de bruit
- Impédance d'entrée très élevée (>10¹⁰ ohms)
- Sortie protégée contre les courts-circuits
- Pour applications faisant appel à une alimentation simple ou double

Valeurs typiques à 25°C:

- Tension d'alimentation: V_{CC} = 0V à +15VDC
- Tension d'entrée différentielle: 30VDC
- Tension d'entrée: 15VDC
- Dissipation de courant: 600 mW
- Temp. de fonctionnement: 0°C à 70°C

POUR PLUS DE DÉTAILS, CONSULTER LES
LIVRES DE DONNÉES RADIO SHACK

TL 074 USED -
SAME PINOUT

RS275-215 DPDT RELAY

275-215

359

RS

Feature

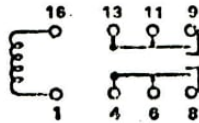
- Fits std. 16 pin IC socket

Absolute maximum ratings

Ambient Temperature: -25°C to +60°C
Continuous Coil Voltage: 7.5VDC
Coil Dissipation: 1W at 20°C

Electrical characteristics

Coil Resistance: 50 ohms $\pm 10\%$
Pull In Voltage: 3.6 VDC



Caractéristique

- Pour douille de CI standard à 16 broches

Valeurs maximales absolues

Température ambiante: -25°C à +60°C
Tension continue de bobine: 7.5 V CC
Dissipation de bobine: 1 W à 20°C

Caractéristiques électrique

Résistance de bobine: 50 ohms $\pm 10\%$
Tension d'amorçage: 3.6 V CC