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Guard-Ring-Free InGaAs/InP Single-Photon Avalanche Diode Based on a Novel One-Step Zn-Diffusion Technique

Ekin Kizilkan, *Student Member, IEEE*, Utku Karaca, *Student Member, IEEE*, Vladimir Pešić, *Student Member, IEEE*, Myung-Jae Lee, *Member, IEEE*, Claudio Bruschini, *Senior Member, IEEE*, Anthony J. SpringThorpe, Alexandre W. Walker, Costel Flueraru, *Senior Member, IEEE*, Oliver J. Pitts, *Member, IEEE*, and Edoardo Charbon, *Fellow, IEEE*

***Abstract*—This work presents a novel InGaAs/InP SPAD structure fabricated using a selective area growth (SAG) method. The surface topography of the selectively grown film deposited within the 70 μm diffusion apertures is used to engineer the Zn diffusion profile to suppress premature edge breakdown. The device achieves a highly uniform active area without the need for shallow diffused guard ring (GR) regions that are inherent in standard InGaAs/InP SPADs. We have obtained 33% and 43% photon detection probability (PDP) at 1550 nm, with 5 V and 7 V excess bias, respectively. These measurements were performed at 300 K and 225 K. The dark count rate (DCR) per unit area at room temperature and at 5 V excess bias is 430 cps/μm^2 and it decreases to 5 cps/μm^2 at 225 K. Timing jitter is measured with passive quenching at 1550 nm as 149 ps at full-width-at-half-maximum (FWHM), (300 K, 5 V excess bias). The proposed technology is suitable for a number of applications, including optical time-domain reflectometry (OTDR), quantum information, and light detection and ranging (LiDAR).**

***Index Terms*—InGaAs/InP, LIDAR, photon counting, single-photon avalanche diodes (SPADs), 3-D ranging, time-correlated single-photon counting (TCSPC), III-V.**

I. Introduction

LOW-LEVEL-LIGHT detection in short-wave-infrared (SWIR) wavelengths with high spatial and timing accuracy is a growing area of interest by the virtue of applications such as quantum information [1], OTDR [2], and LiDAR [3]–[6]. Various device structures have been proposed to target these applications. Superconducting nanowire single-photon detectors have shown remarkable detection efficiency and timing jitter performance, but they require cryogenic temperature operation which limits their application areas [7]–[9]. Ge-on-Si single-photon avalanche diodes (SPADs) have the potential of being integrated within a single chip together with CMOS read-out electronics, but the lattice mismatch between Si and Ge has been a significant challenge delaying the acceptance of such detectors. Recently significant improvement has been shown in the performance of Ge-on-Si SPADs [10], but compared to InGaAs/InP SPADs, they show higher noise and lower operating temperature. Thus, InGaAs/InP SPADs are still the default technology for the applications in SWIR.

This work aims to develop a SPAD pixel that operates at SWIR region to be used in a LiDAR camera. Operating at SWIR wavelengths for LiDAR applications has various advantages such as lower attenuation due to atmosphere, and reduced background noise from black-body radiation of the Sun. Moreover, eye safety limits are higher at SWIR wavelengths [3]. Compared to visible wavelengths, 1550 nm benefits from significantly higher permissible input power. As a result, it is possible to detect objects at a higher distance. In addition to operation wavelength, pixel performance metrics like timing jitter, photon detection probability, noise, and pixel pitch play a crucial role for LiDAR. Therefore, in the proposed structure, low noise pixels with highly uniform PDP throughout the active pixel area are targeted, along with good timing resolution.

There have been significant efforts to improve the performance of InGaAs/InP SPADs through optimizing the Zn diffusion profile, layer dopings and thicknesses [11]–[14]. However, all these designs are based on a standard double diffusion guard ring in which a significant part of the pixel area is not active. Moreover, this type of device usually exhibits enhanced electric field at the device periphery at low excess biases. Some groups have worked on one-step diffusion-based InGaAs/InP SPADs by applying recess-etching [15], [16]. However, their performance is quite low compared to double-diffusion-based ones. In this

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Ekin Kizilkan, Utku Karaca, Vladimir Pešić, Claudio Bruschini, and Edoardo Charbon are with the Advanced Quantum Architecture Laboratory (AQUA), École Polytechnique Fédérale de Lausanne (EPFL), 2000 Neuchâtel, Switzerland (e-mail: ekin.kizilkan@epfl.ch; utku.karaca@epfl.ch; vladimir.pesic@epfl.ch; claudio.bruschini@epfl.ch; edoardo.charbon@epfl.ch).

Myung-Jae Lee is with the Post-Silicon Semiconductor Institute, Korea Institute of Science and Technology (KIST), Seoul 02792, South Korea (e-mail: mj.lee@kist.re.kr).

Anthony J. SpringThorpe, Alexandre W. Walker, Costel Flueraru, and Oliver J. Pitts are with the Advanced Electronics and Photonics Research Centre-National Research Council of Canada, Ottawa, ON K1A 0R6, Canada (e-mail: tony.springthorpe@nrc.ca; alexandre.walker@nrc-cnrc.gc.ca; costel.flueraru@nrc-cnrc.gc.ca; oliver.pitts@nrc-cnrc.gc.ca).

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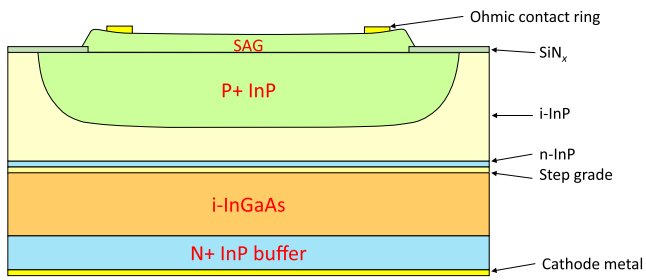


Fig. 1. Schematic of SAG based InGaAs/InP SPAD. Green parts highlight the InP doped by Zn.

work, a novel InGaAs/InP SPAD structure based on SAG is proposed [17]. Edge breakdown is prevented by a single diffusion thanks to the surface topography of SAG epitaxy. Device has a very uniform electric field even at low excess bias. In addition, as the extra area of the GR region is preserved, this approach has the potential of achieving a smaller pixel pitch for the same active area. Thus, it enables larger pixel arrays to reach a better spatial resolution. The SAG topography is also highly reproducible, and does not require frequent tuning. Besides, compared to the double Zn-diffusion technique, the SAG process offers an advantage in the reduced complexity of the diffusion depth calibration, since only one diffusion run needs to be taken into account. Hence, SAG method based InGaAs/InP SPAD technology is a very promising candidate to develop next-generation LiDAR applications.

II. Device Design

A. Device Structure

Device design utilizes lattice-matched In $_{0.53}$ In 0.53Ga $_{0.47}$ Ga 0.47As (hereafter referred to as InGaAs) ternary semiconductor material for photon absorption and InP for avalanche multiplication. The device structure is demonstrated in Fig. 1. This kind of layer structure is referred to as separate absorption, grading, charge, and multiplication (SAGCM) type. It is designed to confine the high electric field required for avalanche multiplication, inside the large bandgap (1.34 eV) InP region, while a modest electric field is formed in the absorber InGaAs region to sweep photogenerated carriers from InGaAs to InP. This is achieved by inserting a narrow n-type doped InP charge sheet. The electric field difference between the absorption and multiplication regions is strictly determined by the doping concentration and the thickness of the charge sheet. A five-step grading layer is grown between charge and absorber layers to ensure a smooth transition in the valance band [18]. The final structure has $\sim$1.8 μm thick i-InGaAs absorber, and $\sim$3 μm thick i-InP cap layers where 2 μm Zn diffusion was performed. 1.8 μm thick i-InGaAs layer allows to absorb almost all the incident light which passes through the absorber two times thanks to the back-side metallization. 1 μm thick multiplication width was selected to keep the tunneling contribution in DCR low whilst not degrading the jitter of the device [19]. Then, the i-InP cap layer was made thick enough for Zn diffusion, and a low field enhancement effect at the device edge is thus obtained by avoiding excessively sharp junction curvature. $\sim$0.1 μm thick n-InP charge layer was doped in the range of 2-2.5 $\times$ 10^{17} cm^{-3} to have 25 V +/$-$5 V difference between the punch-through and breakdown point, which ensures the complete depletion of the absorber. After the epitaxial growth and Zn diffusion process, the back-side of the device is fully covered with Au metal to form the cathode contact. A ring-shaped, ohmic metallization of 5 μm width, and 56 μm inner diameter is then deposited around the periphery of the device for the anode metallization. The active area of the device is therefore partially shaded by the ohmic metal. This design was adopted for ease of testing with front-side illumination; however, for eventual smaller diameter devices or pixelated arrays, a backside-illuminated geometry would be advantageous in order to maximize the anode electrical contact area without causing optical shading.

In standard InGaAs/InP SPADs, a double diffusion technique is used to prevent premature edge breakdown. A deep Zn diffusion defines the active area while a shallow diffusion on the periphery of the device prevents a steep variation of the depletion front. This approach has been proven to be a successful method by many groups for suppressing edge breakdown. However, the area covered by the shallow diffusion increases the device size while it does not contribute to the efficiency of the device. As a result, the fill factor of the device becomes sub-optimal. In the proposed design, edge breakdown is successfully prevented by a single diffusion step thanks to SAG. Prior to Zn diffusion, a $\sim$300 nm thick undoped InP layer was grown by SAG at the center of the device. The thickness of this layer gradually rises from center to mask edge due to enhanced growth rate [20], and it reaches $\sim$700 nm at the device edge. Zn diffuses through the tapered InP surface such that the doping profile inside InP has a steady transition towards the periphery. This ensures that the electric field around the device edge is lower than the center. The diameter of the diffusion window for this particular device is 70 μm. Further details on the device fabrication are explained in [17]. To be able to test the operability of the same process conditions in Geiger mode, and perform detailed active area scanning analysis in a more effective way, in this study, large-diameter devices were selected. The most significant variation in the SAG topography and resulting Zn diffusion depth profile occurs over a length scale of $<\sim$5 μm, thus we can reasonably expect that the process will be applicable to device diameters in the range of 10-15 μm. Demonstration of small device diameters and state-of-the-art pixel pitches thanks to the SAG method is an ongoing future work.

B. Device Simulations

The electrical simulations of the device are performed using Synopsys TCAD commercial software. Doping values measured with the SIMS method given in [21] were used for Zn diffusion, charge, and grading regions. As for the lateral doping profile, the Zn diffusion edge curvature of the simulated device was adjusted to match approximately the curvature seen on the SEM images of the device cross-section from [17]. Regarding the avalanche generation, the quasi-physical model from [22] is first used to calculate the impact ionization coefficients in InP. In the TCAD

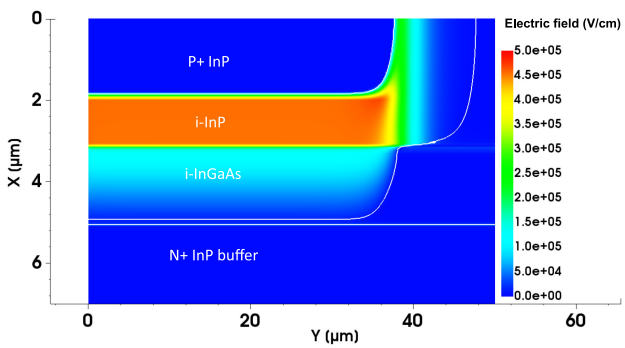


Fig. 2. 2D electric-field simulation of half device at 300 K and at 5 V excess bias.

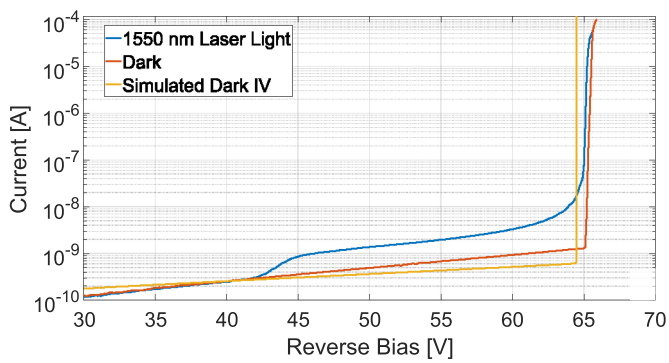


Fig. 3. I-V measurements of SAG-based InGaAs/InP SPAD in dark and under 1550 nm wavelength light illumination together with simulated I-V curve at 300 K.

environment, the Okuto-Crowell model [23] was utilized for the avalanche process, where fitting parameters are adjusted to match ionization coefficients between [22] and TCAD under various electric fields. The simulated breakdown voltages based on this model have presented a good agreement with measured ones from various devices. In Fig. 3 the difference of about 0.5 V between the measured and simulated breakdown voltage arises most probably from a variation in the doping of the charge region. The doping in this region has a strong influence on the breakdown voltage and a variation of only a few percent in this level can cause a noticeable difference in the breakdown voltage. Moreover, a slight difference between simulated and actual multiplication width may also have a contribution in this difference. In order to obtain the I-V curve below breakdown voltage, typical lifetime values for InGaAs [24] and InP [25] materials were plugged in from literature, which are at the order of μs. Then, the surface current was defined between cap i-InP and SiN layers by introducing traps at the interface. Trap locations were assumed to be at the mid-gap position. Trap concentration and cross section were used as fitting parameters to have good matching with experimental I-V.

The electric field distribution of the device at 5 V excess bias and at 300 K is depicted in Fig. 2. It shows that the high electric field is well confined below the diffused region. Moreover, the engineered diffusion front at the periphery is successful in eliminating the edge breakdown. Also, the electric field inside the absorber region has a linear gradient due to n-type background doping. It is kept below 150 kV/cm which is sufficiently low to prevent tunneling noise, and it reaches to 15 kV/cm at the InP buffer interface, which ensures that the absorber is fully depleted [18].

III. Measurement Results

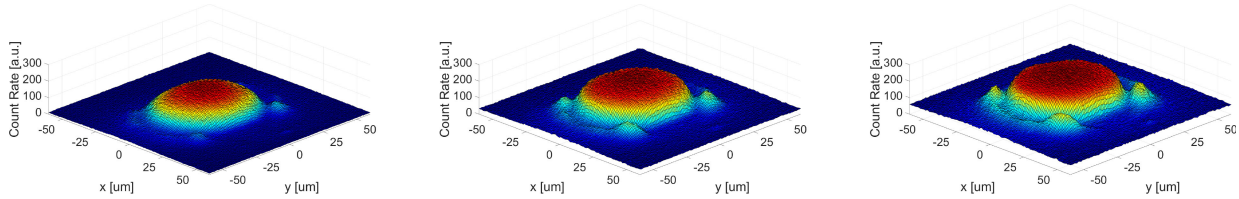
Geiger-mode characterizations were performed in gated mode to suppress afterpulsing at high excess bias voltages. A DC voltage that is 1 V lower than the breakdown voltage of the SPAD was summed with a square pulse of 50 ns duration by utilizing a commercial bias-tee. The summed voltage was applied to the cathode of the device and the output pulse was read from the anode through a 50 kΩ resistor to passively quench the SPAD. The number of pulses are counted by a digital oscilloscope (Teledyne LeCroy WavePro 760Zi-A) connected to the quenching resistor. Temperature sweeps are done by employing a compact liquid nitrogen cooler stage (Linkham LTS420E-P).

A. I-V Characteristics

The I-V curves (acquired by Agilent SMU B2902 A at room temperature) under illumination and dark conditions are depicted in Fig. 3. A 1550 nm laser is used to illuminate the devices and identify the punch-through voltage. Since this wavelength is not absorbed by the InP layer, the voltage at which photocurrent develops indicates that the InGaAs absorber region is depleted. The device shows a sharp avalanche breakdown at 65 V and a punch trough voltage of $\sim$43 V which ensures the absorber region will be depleted for a broad temperature range.

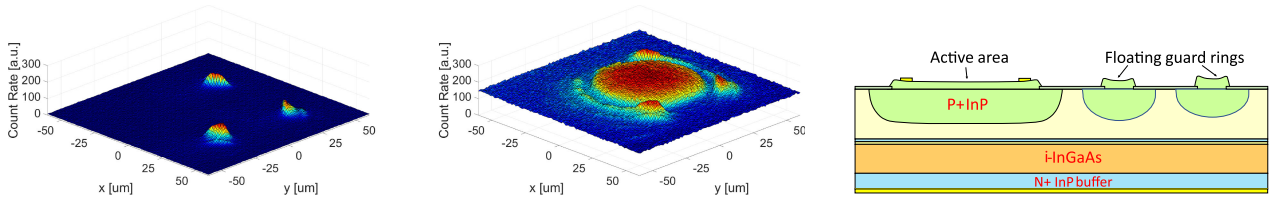
B. Active Area Scan

In order to investigate the uniformity of the electric field within the device, a 1550 nm laser beam is focused on the device through a confocal microscope. The focused light beam was shifted in a window of 120 μm $\times$ 120 μm with a step size of 1 μm and at each beam position, the count rate of the SPAD was recorded. Photomaps are regarded as the examination of the electric field within the device since the regions with a photoresponse are the regions where avalanche multiplication occurs. In addition to the device shown in Fig. 1, another device with two floating GRs was also measured to investigate their impact on device performance. Its cross-section is shown in Fig. 5. Fig. 4 demonstrates the measured 2D photomap of the device without GR at 3, 5, and 7 V excess biases and Fig. 5 shows it for the device with two floating GRs at 3 and 5 V excess biases. A highly uniform response is observed at 3 V excess bias while at 5 and 7 V excess biases anomalous side lobes appear for the device without a GR. The maximum sidelobe to center response ratio at 3 and 5 V excess biases are 55 % and 70% respectively. However, the photoresponse of the device with floating GRs is dominated by the side lobes at 3 V excess bias. At 5 V excess bias, the field at the sidelobe saturates, as a result the peak responses at the center and the sidelobes become similar. In agreement with the photocurrent maps reported here [17], sidelobes occur along [100] and [010] crystal directions. The



(a) 3 V excess bias (b) 5 V excess bias (c) 7 V excess bias

Fig. 4. Active area scans of the device without GR under focused 1550 nm laser light at 300 K.



(a) 3 V excess bias (b) 5 V excess bias (c) Schematic of the device with floating GR

Fig. 5. Active area scans of the device with two floating GRs under focused 1550 nm laser light at 300 K. The scan could not be performed at 7 V excess bias due to high DCR that is probably arising from the high electric field on the sidelobes. While there are also floating guard rings on the left side of the device, they are not shown in the schematic.

uniformity of the SAG surface around the mask edge was disturbed along these directions which resulted in a deeper Zn diffusion and enhanced electric field. The SAG process achieves edge effect suppression by relying on the growth enhancement at the edge of the device, which is driven by near-surface diffusion of the growth precursors over the masked areas of the wafer [26]. In the floating GR devices, this growth enhancement is most pronounced in the outermost open areas, which are the floating GRs, with less growth enhancement at the edge of the active area compared to non-floating GR devices. This may be the reason for less effective suppression of edge enhancement for the floating GR devices, which in this case manifests itself in the anomalous lobe features observed along specific directions at the edge of the device. Finally, the effective active area is calculated for the scan results in Fig. 4 by integrating the regions which have a response higher than the half maximum. Calculated diameters based on the effective active area are 53 μm, 59 μm, and 63 μm at 3, 5, and 7 V excess biases respectively. Partial shading induced by the anode metallization is visible as a blue region in Fig. 5(b) between the center active region and sidelobes.

C. Noise Performance

The noise floor of a SPAD determines the minimum distinguishable photon rate incident on the device. Pulses that appear in the absence of light presence establish the noise of a SPAD. Primary dark pulses appear due to intrinsic carrier generation in bulk semiconductor, and secondary dark pulses occur as trapped charges from a previously triggered avalanche escape the trap confinement potential over a longer time constant. The former is referred to as primary DCR while the latter is called afterpulsing. The main generation mechanisms that contribute to DCR are Shockley-Read-Hall (SRH) from InGaAs and trap-assisted tunneling (TAT) from InP. SRH is highly correlated to crystal quality and TAT generation can be enhanced in regions of high electric field. Afterpulsing is a dominant process for InGaAs/InP SPADs and it is usually controlled by limiting the amount of charge flowing during avalanche current generation and keeping the SPAD below breakdown voltage until all the trapped carriers are released.

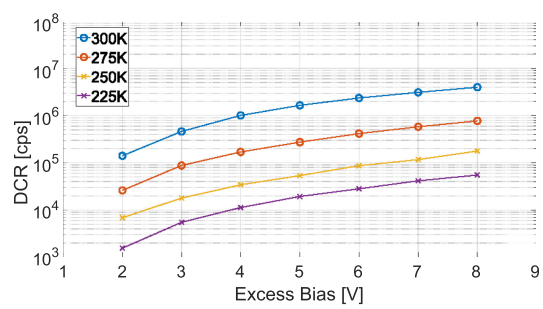


Fig. 6. DCR measurement of the device without GR from 225K-300 K and 2 V-8 V.

1) Dcr: Measurements of primary DCR are realized at a gate-off time of 250 μs to neglect afterpulsing. Results with respect to excess bias for a temperature range of 225K-300 K are plotted in Fig. 6 and Fig. 7. The device without GR demonstrates a DCR of 20 kcps at 225 K and 5 V excess bias. At room temperature, DCR reaches up to 1.6 Mcps due to thermal generation in the absorber region.

The device with GR has shown DCRs that are about one order of magnitude higher than guard ringless device at all temperatures. A more clear DCR comparison of the two devices can be found in Fig. 8. As highlighted, at 3 V excess bias while only small sidelobes are active for the device with floating GRs, its DCR reaches the level of the one without GR. In other words, the DCR contribution of the small sidelobes is comparable to the

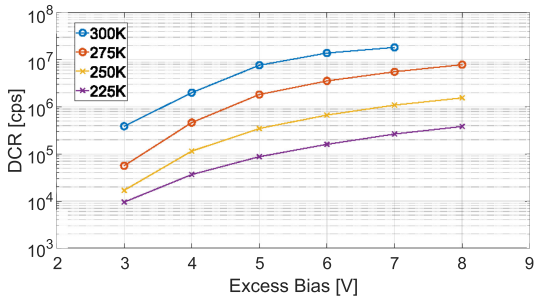


Fig. 7. DCR measurement of the device with two floating GRs from 225K-300 K and 3 V-8 V. Due to count rate saturation at 8 V excess bias at 300 K, the result is not plotted at this particular point.

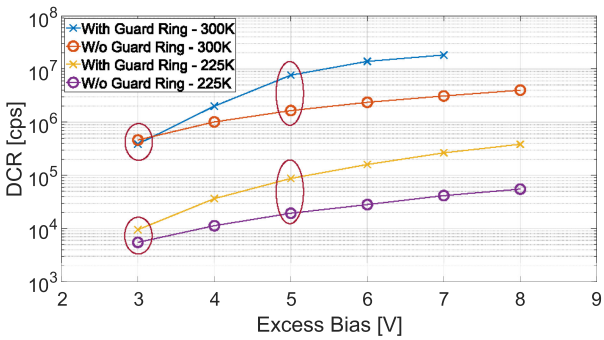


Fig. 8. DCR results of both devices at 225 K and 300 K. Values at 3 V and 5 V excess bias are highlighted.

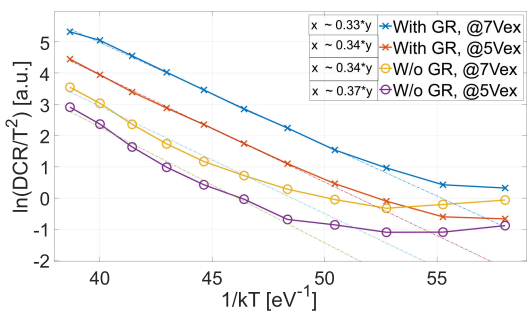


Fig. 9. Activation energy curves of both devices at 5 V and 7 V excess biases.

DCR arising from the entire active area of the device without GR. At 5 V excess bias, when the center regions of both devices are active, the DCR ratio of the two devices becomes ∼4 which indicates that a significant part of the DCR of the device with GR results from the enhanced electric field at the sidelobes. This is further investigated by activation energy curves. Under the assumption that SRH generation is the dominant primary DCR source, the relation between DCR and temperature can be described as

$$DCR \quad \propto \quad T^2 \cdot e^{\frac{-E_a}{kT}}, \tag{1}$$

where E_a is the activation energy and k is Boltzmann's constant [27]. Activation energies at 5 and 7 V excess biases are obtained by plotting $\ln(DCR/T^2)$ $vs.$ $1/kT$ and fitting a linear curve as in Fig. 9. An activation energy of 0.37 eV is measured

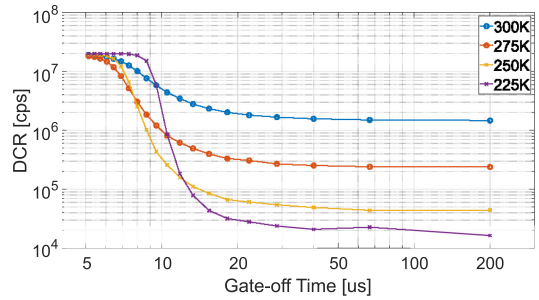


Fig. 10. DCR $vs.$ Gate-off time for the device without GR at 50 ns gate-on time and at 5 V excess bias.

at 5 V excess bias for the device without GR. This energy level corresponds to the half bandgap of InGaAs and indicates dominant DCR mechanism down to 230 K is SRH generation in the absorber region. On the other hand, the activation energy for the device with GR is 0.34 eV (<0.37 eV) at 5 V excess bias. That indicates the DCR is not solely dominated by the SRH mechanism but instead is a combination of SRH and TAT. Activation energies decrease also at 7 V excess bias due to enhanced electric field for both devices.

It should be noted that sidelobes reach a response level that is comparable to the center of the device without GR at 7 V excess bias. DCR generated at these sidelobes is degrading the device performance. Thus, there is some room to improve the DCR of the device without GR by optimizing the SAG process to eliminate sidelobes.

2) Afterpulsing: Ruling out the contribution of afterpulsing to primary DCR and PDP is an important aspect for accurate characterization of the device performance. Afterpulsing could result in overestimation of DCR and PDP as it can cause higher count rates. A reliable method to ensure afterpulsing is fully eliminated is to use a long enough gate-off time such that all traps are released. Fig. 10 shows the DCR $vs.$ gate-off time at temperatures from 225 K to 300 K. At all temperatures, there is an increase in DCR for the gate-off times shorter than 20 μs. The increase is sharper for lower temperatures due to enhanced trap lifetimes. The point of increase in DCR strongly depends on the number of trapped carriers which is proportional to the charge that is flowing during an avalanche. Moreover, the amount of charge is affected by pulse duration. Therefore, a shorter gate-on time would result in a shift in the curve towards a shorter gate-off duration. At long gate-off times, DCR does not vary, meaning afterpulsing does not impact the count rate. Therefore, 250 μs gate-off time at 50 ns is used for PDP measurement similar to primary DCR measurements.

D. Photon Detection Probability

PDP measurements were performed based on the setup shown in Fig. 11. A laser pulse of length ∼40 ps at 1550 nm wavelength is utilized. Laser pulse and electrical gate are synchronized by the waveform generator such that photons reach the SPAD while its voltage is above breakdown. Light power is divided through a beam splitter such that high output end is connected to a power meter to calculate the number of photons incident on the device.

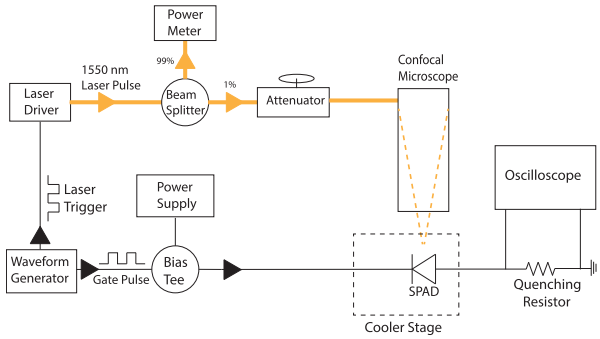


Fig. 11. Schematic of PDP measurement setup.Black lines show electrical connections while yellow ones correspond to the optical path.

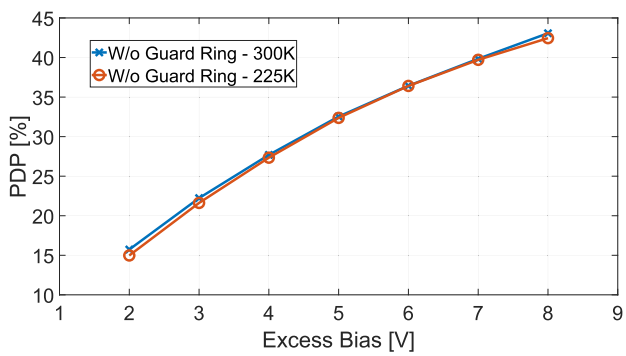


Fig. 12. PDP measurement results of the front-illuminated device without GR at 225 K and 300 K (1550 nm).

Power at the low output end is attenuated further and focused on the SPAD by the confocal microscope. The main advantage of a PDP measurement with a focused beam is that ambiguity on the active area is avoided. When PDP is measured by illuminating the entire chip area, inaccuracies in estimating the active device area could impact the result significantly [13]. Moreover, charge persistence could cause uncertainty in the active area especially at low temperatures [12], [28], [29]. PDP is calculated by the equation

$$PDP = \frac{1}{\mu} \cdot ln \left[\frac{1 - C_d/f}{1 - C_t/f} \right], \quad (2)$$

where C_d stands for the number of dark counts per second, C_t for the total number of counts per second under illumination, f is the gate frequency, and μ is the average number of photons per optical pulse [27]. A PDP of 32% was measured at an excess bias of 5 V, while at 7 V, it grew to 43% as shown in Fig. 12. Measured PDP values do not vary significantly at 225 K and 300 K consistently with literature [27]. PDP rises as excess bias increases due to the enhanced electric field in the avalanche region and higher breakdown probability. However, PDP saturates as impact ionization coefficients saturate at high excess bias [30].

E. Timing Jitter

Timing jitter is a critical performance metric that impacts the depth accuracy for LiDAR applications. The setup depicted

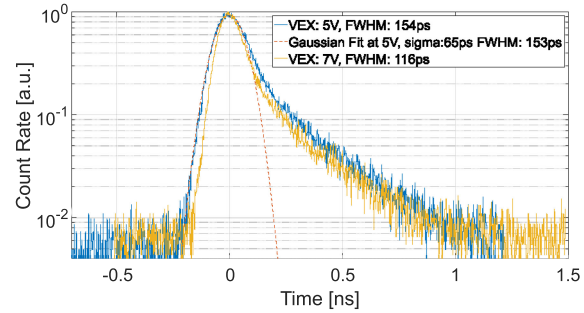


Fig. 13. Jitter measurement results at 5 V and 7 V excess bias. Measurements were done with a focused 1550 nm picosecond pulsed laser at 300 K.

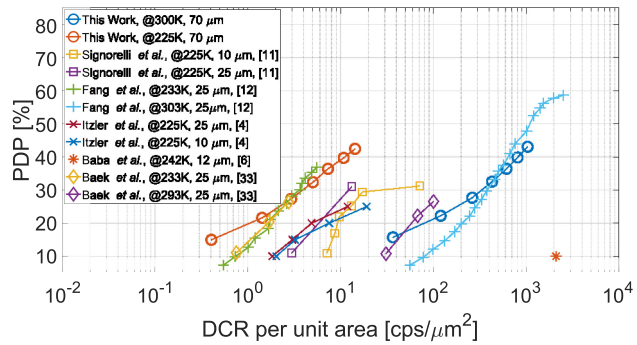


Fig. 14. Comparison of DCR and PDP to state-of-the-art.

in Fig. 11 was also used for jitter measurement with slight modifications. A reference signal to mark photon arrival is connected to the oscilloscope. Then a histogram of the time differences between the avalanche pulse and the reference signal is produced by the oscilloscope. Measurements were performed at room temperature, 1550 nm wavelength, in single-photon regime. Jitter results are 154 ps and 116 ps at FWHM at 5 and 7 V excess bias as depicted in Fig. 13. Calculated FWHM values include the effect of the laser pulse width. The actual timing jitter of the device is obtained as 149 ps and 109 ps after deconvolution with 40 ps of optical pulse. Fig. 13 also shows the jitter result at 5 V excess bias and the Gaussian fit with a standard deviation of 65 ps. Measured diffusion tails for 5 and 7 V excess bias are 110 ps and 92 ps respectively. Compared to the result reported in [11], the diffusion tail observed from the device in this work is longer. This is probably because of the thicker InGaAs absorber region utilized in this work. Thicker InGaAs region results in larger ambiguity in the transit times of the photo-generated carriers from absorber region to multiplication region. It is worth mentioning that jitter measurements using a focused beam instead of wide-area illumination can cause a better estimation of the jitter due to eliminated lateral diffusion as reported here [13]. On the other hand, employing a good sensing circuit with a low threshold and reduced parasitic capacitance may enhance jitter performance [31], [32].

IV. Comparison With the State-of-The-Art

Fig. 14 and Table I shows the comparison of DCR per unit area and PDP of our work with state-of-the-art devices. DCR per

TABLE I
SUMMARY AND COMPARISON OF SPAD PERFORMANCE

Reference	Temperature [K]	Active Diam. [μ]	PDP [%] @ 1550 [nm]	DCR / area [cps / μm^2] @ PDP [%]	DCR [cps] @ PDP [%]	Jitter [ps] @ PDP [%]
This Work	300	70	15 - 43	36.7 - 1 k @15 - 43	141 k - 4 M @15 - 43	149 - 109 @32 - 43
	225	70	15 - 43	0.4 - 14.4 @15 - 43	1.6 k - 55 k @15 - 43	N.A.
Itzler *et al.* [4]	225	10	10 - 25	2 - 19 @10 - 25	160 - 1.5 k @10 - 25	N.A.
	225	25	10 - 25	1.8 - 12 @10 - 25	900 - 5.8 k @10 - 25	N.A.
Baba *et al.* [6]	242	12	10	2.1 k @10	234 k @10	260[a]
Signorelli *et al.* [11]	225	10	11 - 30	7 - 71.5 @11 - 30	560 - 1.4 k @11 - 30	225 - 84 @11 - 30
	225	25	11 - 30	2.98 - 13.2 @11 - 30	1460 - 6.5 k @11 - 30	340 - 119 @11 - 30
Fang *et al.* [12]	303	25	7 - 60	55.9 - 2.5 k @7 - 60	27 k - 1.24 M @7 - 60	N.A.
	233	25	7 - 37	0.5 - 5.5 @7 - 37	260 - 2.5 k @7 - 37	N.A.
Baek *et al.* [33]	293	25	11 - 27	31 - 100 @11 - 27	15 k - 50 k[b] @11 - 27	N.A.
	233	25	11 - 27	0.8 - 2.8 @11 - 27	370 - 1.4 k[b] @11 - 27	N.A.

[a]Performed at @ 1.6 V_{EX}. [b]Calculated from dark count probability and 2 ns pulse width.

unit area is preferred as comparison metric of noise since DCR is proportional to device area. The highest PDP was achieved at the lowest DCR per unit area at 225 K. This temperature can be reached with a peltier cooling and a hermetic package. Performance comparison at room temperature is also investigated due to interest in LiDAR applications. At this temperature, the devices reported here reach a similar performance as [12] in terms of noise. The importance of active area uniformity and its impact on the noise are discussed in sections B and C by comparing the devices with and without GR. Device designs that utilize double diffusion usually show higher response around the edge until excess bias reaches 5 V [13], [19], [34]. One of the remarkable features of SAG-based InGaAs/InP SPAD is that, with only one-step Zn-diffusion, avalanche generation is well confined at the device center even at 3 V excess bias. Reducing these edge effects is likely the reason such a low DCR per unit area is achieved. Thanks to the minimized contribution of the edges to DCR, a very small change in our DCR per unit area is expected while shrinking the device size as DCR should scale linearly with the device area.

V. CONCLUSION

In this work, a novel InGaAs/InP structure is reported. SAG-based diffusion approach achieves a uniform electric field in the avalanche region with a single diffusion step. Devices reported here show one of the highest efficiencies in SWIR with minimal noise. The pixel photoresponse is also very uniform, and does not show significant edge field enhancement. A GR-free structure would provide a path toward a higher pixel fill factor for future high-density arrays. Furthermore, it can operate at room temperature. All these results indicate that SAG-based SPAD is one of the best candidates for a LiDAR camera thanks to their reproducibility and scalability to large arrays. In future work, pixel sizes will be scaled down while Zn diffusion and SAG thickness will be optimized for the best performance, and SPAD arrays will be fabricated with minimum pixel pitch to be utilized in LiDAR applications.

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Ekin Kizilkan (Student Member, IEEE) received the B.S. degrees in electrical and electronics engineering and in physics from Middle East Technical University, Ankara, Turkey, in 2016 and 2017, respectively, the M.S. degree from École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, in 2019. Since 2019, he has been working toward the Ph.D. degree with Advanced Quantum Architecture Laboratory. From 2016 to 2017, he was a full-time Research Assistant with Quantum Devices and Nanophotonics Research Laboratory, for the design and fabrication of SWIR Cameras based on III/V compound semiconductors. He has been conducting research on single-photon avalanche diodes based on various technologies, such as CMOS, Germanium on Silicon PIC, and III/V to enhance SPADs performance in NIR wavelengths as part of his Ph.D. work.

Utku Karaca (Student Member, IEEE) received the B.S. and M.S. degrees from the Department of Electrical and Electronics Engineering, Middle East Technical University, Ankara, Turkey, in 2016 and 2018, respectively. Since 2019, he has been working toward the Ph.D. degree with Advanced Quantum Architecture Laboratory (AQUA). From 2016 to 2018, he was a Research Engineer with Quantum Devices and Nanophotonics Research Laboratory, for the design, fabrication, and characterization of III-V materials based infrared sensor arrays. He has been conducting research on single photon avalanche diodes based on various technologies, such as CMOS, Germanium/Silicon, and III-V to enhance SPADs performance in NIR and SWIR wavelengths with AQUA.

Vladimir Pešić (Student Member, IEEE) received the B.S. degree in electrical engineering and computer science from the Faculty of Electronic Engineering, University of Niš, Niš, Serbia, in 2019, and the M.S. degree in electrical and electronics engineering from École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, in 2021. He is currently working toward the Ph.D. degree with Advanced Quantum Architecture Laboratory. His research interests include InGaAs/InP SPADs for infrared detection and cryogenic circuits for qubit control and quantum computing.

Myung-Jae Lee (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2006, 2008, and 2013, respectively. His doctoral dissertation concerned silicon avalanche photodetectors fabricated with standard CMOS/BiCMOS technology. From 2013 to 2017, he was a Postdoctoral Researcher with the Faculty of Electrical Engineering, Delft University of Technology, Delft, The Netherlands, where he worked on single-photon sensors and applications based on SPADs. In 2017, he joined the School of Engineering, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland,, as a Scientist, worked on advanced single-photon sensors/applications and coordinating/managing several research projects as a Co-Principal Investigator. Since 2019, he has been a Senior Research Scientist with the Post-Silicon Semiconductor Institute, Korea Institute of Science and Technology, Seoul, South Korea, where he has led the research and development of next-generation single-photon detectors and sensors for various applications. His research interests include photodiodes/photodetectors, single-photon detectors/sensors, and since 2006 concentrating on CMOS-compatible avalanche photodetectors and single-photon avalanche diodes and applications thereof, such as LiDAR, D-ToF, 3D vision, biophotonics, quantum photonics, space, security, silicon photonics, and optical interconnects.

Claudio Bruschini (Senior Member, IEEE) received the Laurea degree in physics from the University of Genova, Genoa, Italy, in 1992, and the Ph.D. degree in applied sciences from Vrije Universiteit Brussel, Brussels, Belgium, in 2002. He is currently a Scientist and Lab Deputy with Advanced Quantum Architecture Laboratory (AQUA), École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland. He has authored or coauthored more than 130 articles and conference proceedings and one book. His scientific interests include high energy physics and parallel computing in the early days, challenging sensor applications in humanitarian demining, and since 2003 concentrating on quantum photonic devices, high-speed and time-resolved 2D/3D optical sensing, and applications thereof (biophotonics, nuclear medicine, basic sciences, security, and ranging). He was the co-recipient of the 2012 European Photonics Innovation Award and Image Sensors Europe 2019 Award in the category Best Academic Research Team, and Swiss Medtech Award 2016 finalist. He is an SPIE Senior Member and Co-founder of a start-up commercialising selected AQUA lab SPAD designs.

Anthony J. SpringThorpe received the B.Sc. degree in physics and the Ph.D. degree in solid state physics from The University of Sheffield, Sheffield, U.K., in 1963 and 1967, respectively. Thereafter, he had a three year postdoctoral fellowship with the University of Bath, Bath, U.K. He was with Northern Electric R&D Labs, later Bell-Northern Research, and then Nortel Networks from 1969 to 2002, where he was responsible for liquid phase epitaxial growth techniques for the preparation of III-V compound semiconductors, built the first Canadian MOCVD system in 1978, and was a Manager of epitaxy from 1978 to 1997. From 1997 to 2002, he was the New Materials Advisor in the High Performance Optical Components division. Since 2002, he has been a Principal Research Officer with the Canadian Photonics Fabrication Centre, National Research Council of Canada, leading its MOCVD Epitaxy Group. Dr. SpringThorpe was the recipient of the 1977 W. Lash Miller prize of the Electrochemical Society, 1999 Nortel President's Prize for technology cascade, 2005 Canadian Association of Physics medal for his contributions to industrial physics, was named MBE innovator of the year by the 2005 North American MBE conference for his contributions to in-situ monitoring techniques for molecular beam epitaxy, and 2007 Lifetime Achievement Award of the Canadian Semiconductor Technology Conference.

Alexandre W. Walker received the B.Sc. degree in astrophysics from Queen's University, Kingston, ON, Canada, in 2007, and the M.Sc. and Ph.D. degrees in physics from the University of Ottawa, Ottawa, ON, Canada, in 2008 and 2013, respectively. From 2013 to 2016, he was a Research Scientist with the Fraunhofer Institute for Solar Energy Systems, Freiburg, Germany, focusing on photovoltaics for space applications. Since 2016, he has been a Research Officer with Advanced Electronics and Photonics Research Centre, NRC, and in 2018 he became an Adjunct Professor with the Department of Physics, University of Ottawa. He has authored or coauthored more than 60 articles and conference proceedings, and holds three patents. His research interests include imaging in the short-wave infrared, single photon detection for LiDAR, photon power converters for wireless power transmission, and next generation sensors for high radiation environments.

Costel Flueraru (Senior Member, IEEE) received the M.S. degree in engineering physics and the Ph.D. degree in physics from the University of Bucharest, Bucharest, Romania. During the Ph.D. program, he conducted research with Applied Optics Group, Department of Applied Physics, University of Twente, Enschede, The Netherlands. He was a Postdoctoral Fellow with the Max Planck Institute for Interfaces and Colloids, Berlin, Germany, and the University of Potsdam, Potsdam, Germany, where he investigated the nonlinear optical properties of organic materials. He was a Visiting Fellow with the Steacie Institute for Molecular Science, National Research Council (NRC), Ottawa, ON, Canada, before joining the Optics Group, Institute for National Measurement Standards, NRC, in 2001. He is currently a Leader of System Integration and Prototyping Group, Advanced Electronics and Photonics, NRC. He is the author or coauthor of more than 60 journal publications and more than 60 conference articles. His research interests include optical sensors and instrumentations, imaging, optical interferometry with applications in optical coherent tomography. Dr. Flueraru is a Senior Member of the IEEE Instrumentation and Measurement Society. He is also a Registered Professional Engineer in the Province of Ontario.

Oliver J. Pitts (Member, IEEE) received the B.Sc. degree in earth and planetary sciences from McGill University, Montreal, QC, Canada, in 1996, and the Ph.D. degree in physics from Simon Fraser University, Burnaby, BC, Canada, in 2004. Thereafter, he held a postdoctoral research with Simon Fraser University and the University of Wisconsin-Madison, Madison, WI, USA, focused on the epitaxial growth of semiconductor materials by MOCVD. In 2009, he joined the MOCVD Epitaxy Group of the Canadian Photonics Fabrication Centre, National Research Council (NRC) of Canada, where he led the development of Zn diffusion processing using the MOCVD reactor. Since 2018, he has been with Advanced Technology Fabrication Group, NRC, concentrating on the design, epitaxial growth and fabrication of III-V photodetectors and imaging arrays, and applications thereof in LiDAR and in optical satellite communications.

Edoardo Charbon (Fellow, IEEE) received the Diploma degree in electrical engineering and EECS from ETH Zurich, Zurich, Switzerland, in 1988, the M.S. degree in electrical engineering and EECS from the University of California at San Diego, San Diego, CA, USA, in 1991, and the Ph.D. degree in electrical engineering and EECS from the University of California at Berkeley, Berkeley, CA, USA, in 1995. From 1995 to 2000, he was with Cadence Design Systems where he was the Architect of the company's initiative on information hiding for intellectual property protection. In 2000, he joined Canesta Inc., as the Chief Architect, where he led the development of wireless 3-D CMOS image sensors. Since 2002, he has been a Member of the Faculty with École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland. From 2008 to 2016, he was with TU Delft, Delft, The Netherlands, as the Chair of VLSI design. Since 2015, he has been the driving force behind the creation of deep-submicron CMOS SPAD technology, which is mass-produced and currently in telemeters, proximity sensors, and medical diagnostics tools. He has authored or coauthored more than 400 papers and two books, and he holds 23 patents. His research interests include 3-D vision, LiDAR, FLIM, FCS, NIROT, super-resolution microscopy, time-resolved Raman spectroscopy, and cryo-CMOS circuits and systems for the control of qubit arrays in quantum computers. Dr. Charbon is a Distinguished Visiting Scholar of the W. M. Keck Institute for Space at Caltech, a Fellow of the Kavli Institute of Nanoscience Delft, and a Distinguished Lecturer of the IEEE Photonics Society.