Digital lighthouse remote control

Vachon, F.

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DIGITAL LIGHTHOUSE REMOTE CONTROL

- F. VACHON -

OTTAWA

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ABSTRACT

A digital remote control system, capable of turning eight latching relays ON or OFF at each of eight different locations from one transmitter, is described. Multisampling of each bit and a digital servo for bit-timing recovery are incorporated. Each 8-bit command has to be received correctly at least five consecutive times before a relay will operate. This makes it virtually impossible for noise to operate a relay falsely.

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DIGITAL LIGHTHOUSE REMOTE CONTROL

– F. Vachon –

Introduction

This digital system was designed to turn lighthouse equipment ON or OFF remotely by a radio link. Eight latching relays may be operated at each of eight different locations by one transmitter. The circuitry is about 90% integrated circuits and 10% discrete components.

Description of Transmitting End

Two different laboratory built radio links have been used to operate the system from the Radio Field Station to the Radio and Electrical Engineering building, a distance of seven miles. The first link that was tried used a 1792 kHz 10-watt transmitter. The results were very good in the daytime, but deteriorated at night because of interference from radio stations. The second link at 225 MHz with a 120-milliwatt transmitter gave good, consistent results. The transmitter was keyed ON and OFF (modulated) by the logic circuitry shown in photographs 1 and 2 and in Figs. 1 and 3.

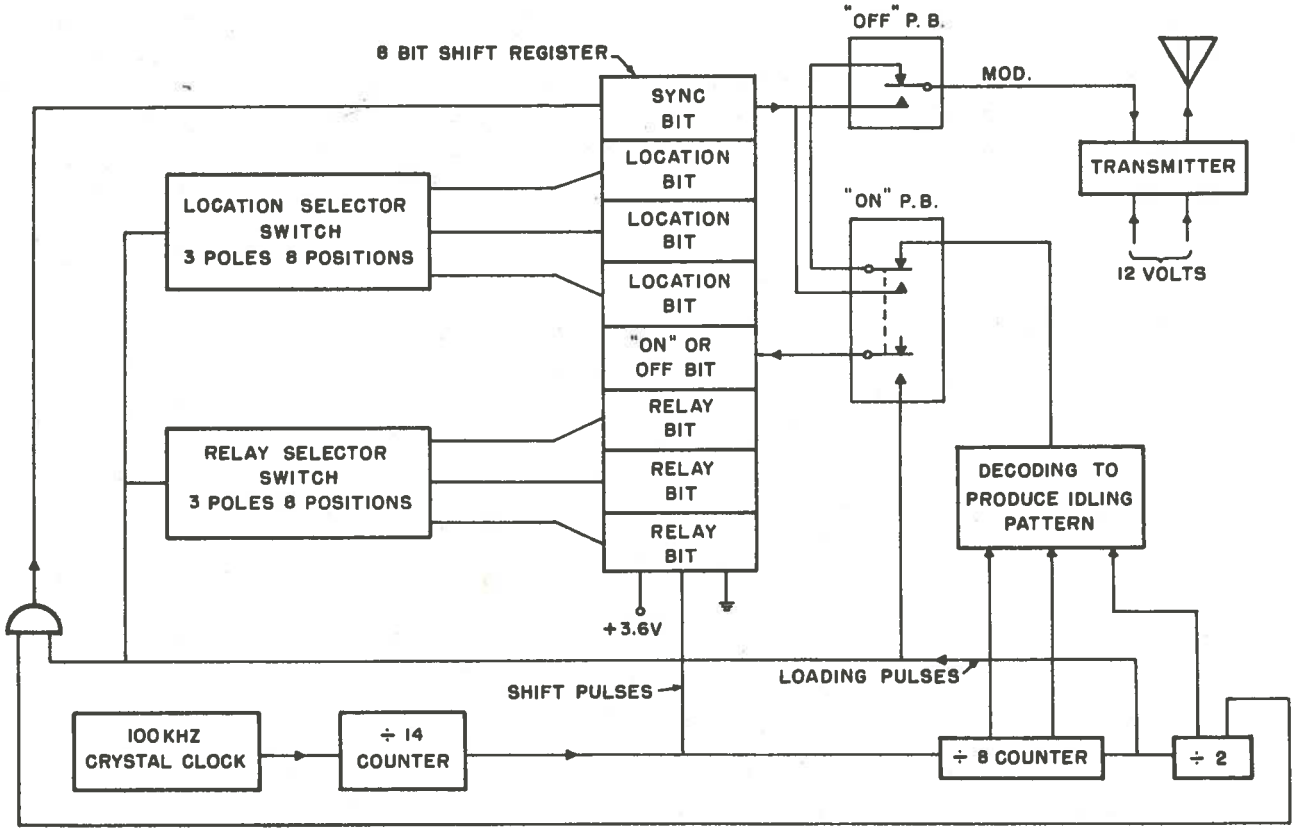


Figure 1 Block diagram – transmitting end

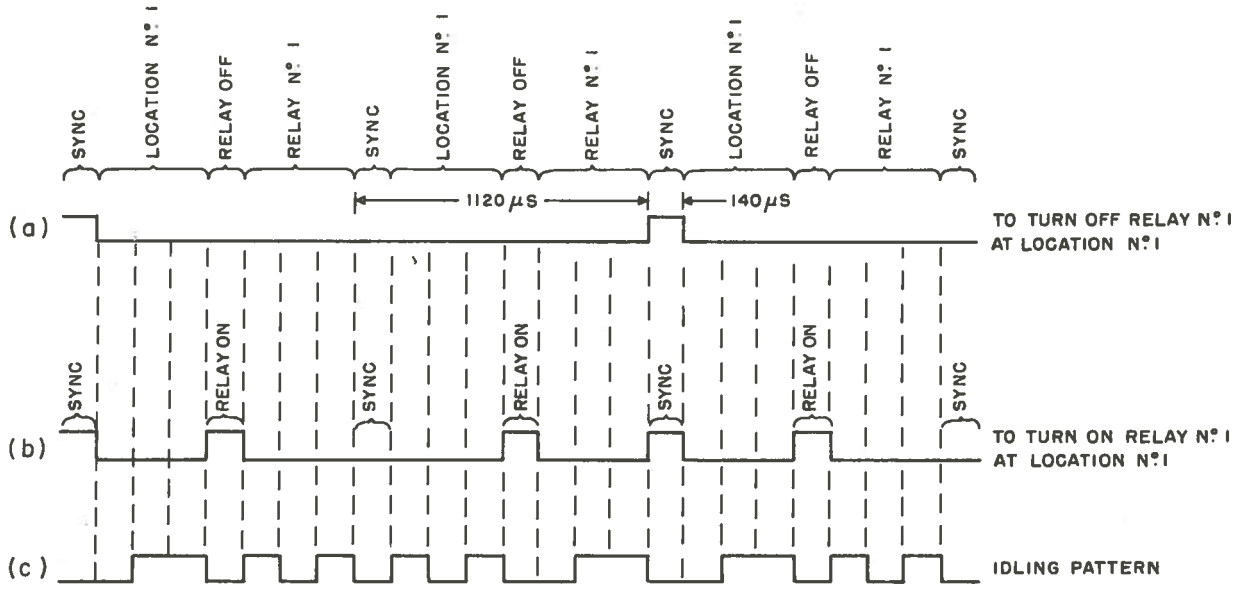


Figure 2 Typical modulation waveforms

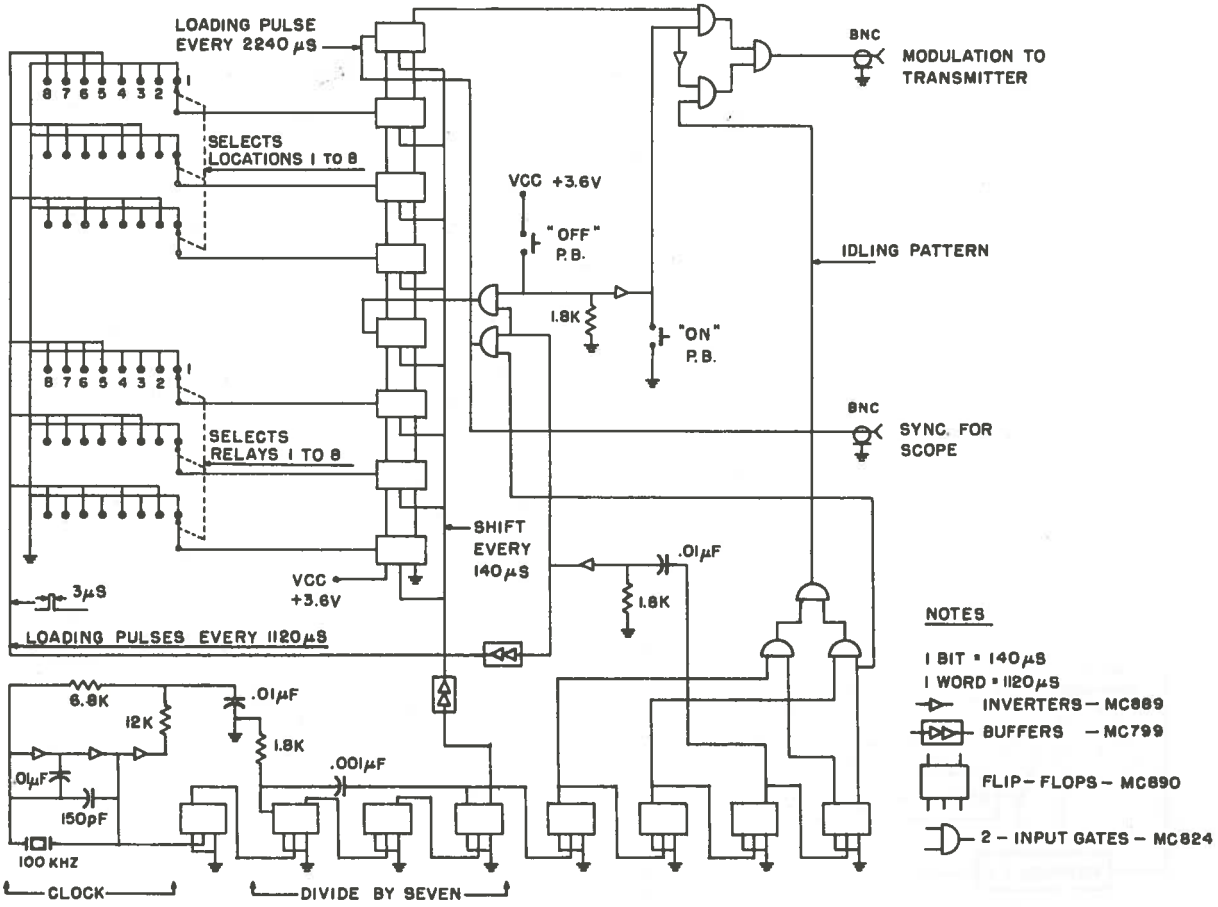


Figure 3 Logic circuitry for modulator

Typical modulation patterns are shown in Fig. 2. Patterns (*a*) and (*b*) will turn on and off relay No. 1 at location 1; as can be seen, the patterns are composed of an endless series of 8-bit words. The words of one pattern are all identical except for the first bit of each word. This is a sync bit which alternates between a 1 and a 0. A 1 turns the transmitter on and a 0 turns it off. The second, third, and fourth bits indicate the location number and are selected by turning an eight-position switch to the desired location. The fifth bit indicates that the relay is to be turned ON if it is a 1 and OFF if it is a 0. This bit is selected by push-buttons. The last three bits indicate the relay number and are again selected by an eight-position switch.

When none of the push-buttons are depressed, a modulation pattern is produced as shown in Fig. 2(*c*). This pattern (idling pattern) cannot operate any relays. It is transmitted to keep the power on and to maintain bit-timing at the receiving end between commands. If the ON push-button is depressed, the pattern changes from (*c*) to (*b*) (if location 1, relay 1, has been selected). If the OFF push-button is depressed the pattern changes to (*a*).

The shift register is shifted every 140 μsec by a crystal-controlled clock. After 8 shifts the register contains all 0's regardless of what was in it initially. Therefore, only the 1's of any code word need to be loaded, every 1120 μsec (every word), into the appropriate flip-flops as determined by the switches. Loading pulses are produced by dividing the shift pulses by 8. A further division by 2 provides pulses every 2240 μsec to load a 1 into the sync flip-flop on every second word only.

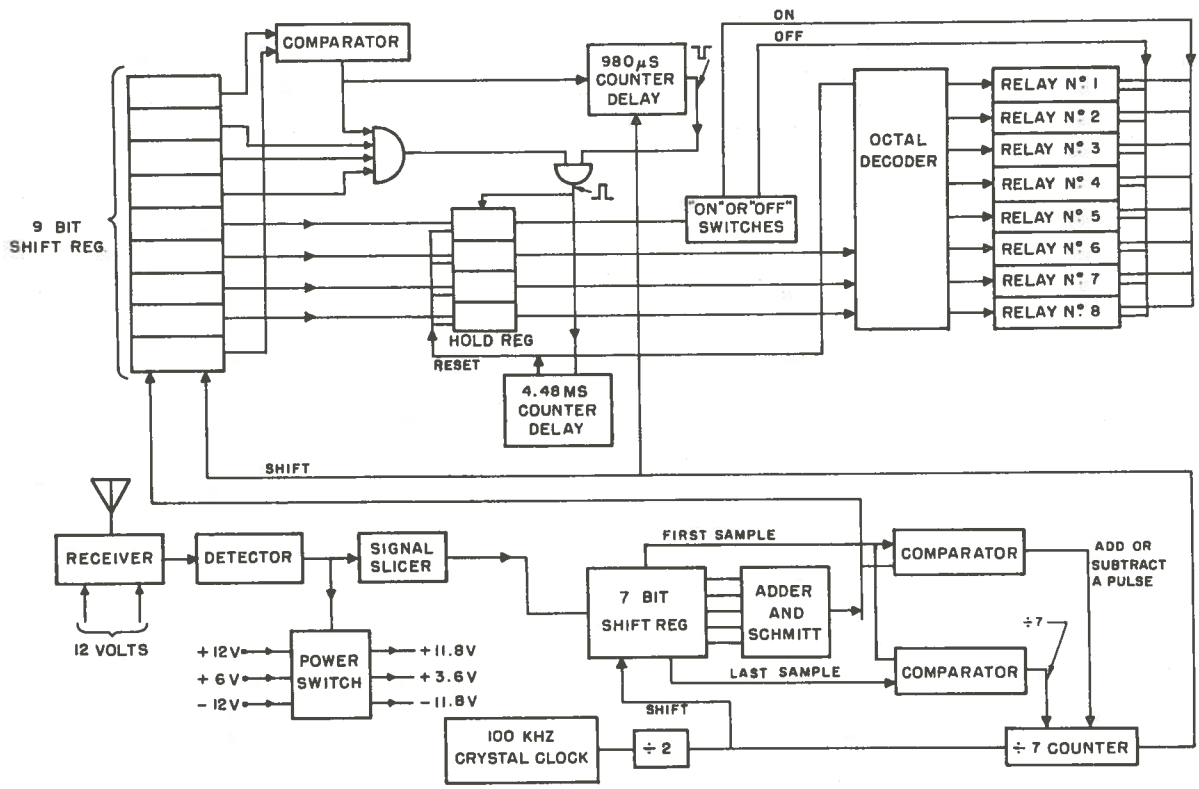


Figure 4 Block diagram – receiving end

Receiving End

Figure 4 shows the block diagram of the receiving end at one location only. It can be divided into four sections for description –

(1) Receiver and signal conditioner
(2) Digital servo for bit-timing recovery
(3) Logic circuitry and decoding
(4) Relays and relay drivers.

Receiver and Signal Conditioner

The circuit diagram of this portion is shown in Fig. 5 and waveforms are shown in Fig. 6 (*a*–*h*).

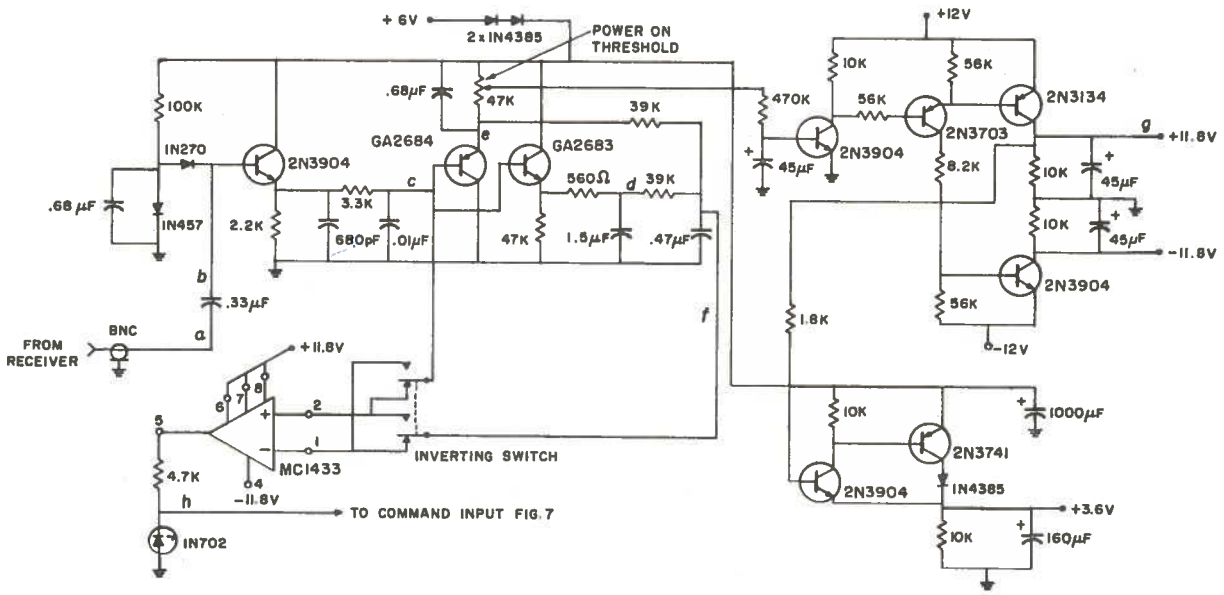


Figure 5 Signal conditioner and power switches

The detected output of the receiver (*c*) is connected to one input of an operational amplifier and to two emitter followers. One emitter follower charges a capacitor with a long time constant (*d*) to the maximum value of the detected waveform, and the other emitter follower charges another capacitor with a long time constant (*e*) to the minimum value of the detected waveform. Two 39-kΩ resistors are connected in series between the two capacitors, and the midpoint of the resistors (*f*) is connected to the other input of the operational amplifier. Thus the detected signal is sliced in the middle and squared up by the operational amplifier (*h*).

The voltage on the minimum capacitor (*e*) turns the power on for the rest of the circuitry. This prevents battery drain when no signal is being received.

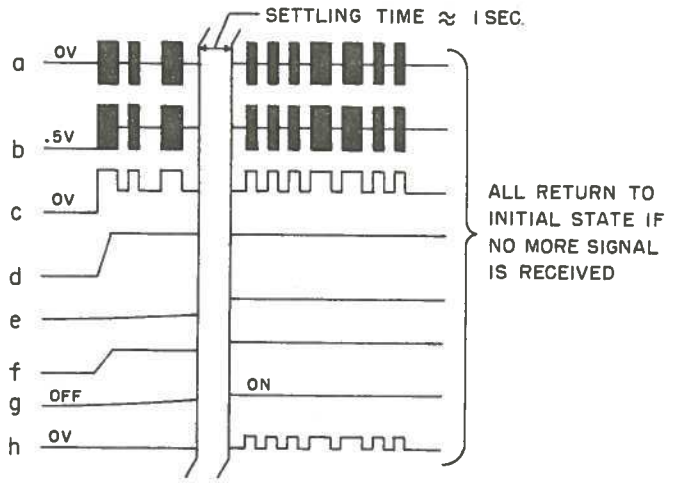


Figure 6 Signal conditioner – waveforms; (a) = undetected receiver output (IF), (c) = (a) after detection, (d) = maximum of (c), (e) = minimum of (c), (f) = average of (d) and (e), (g) = power on or off, (h) = output of operational amplifier

Digital Servo for Bit-Timing Recovery

The circuit diagram and waveforms are shown in Figs. 7 and 8, respectively. This circuit recovers bit-timing by locking locally produced sampling pulses to the received command waveform (Fig. 6 (*h*)). Each bit is sampled seven times for more reliability and the samples are added to decide whether the bit is a 1 or a 0. Bit-timing recovery and multisampling are combined in this circuit.

The circuit consists of the following.

(1) A crystal controlled oscillator to produce a square wave whose period is 1/7 the bit-time of the received data.

(2) A shift register composed of J–K flipflops 1 to 7 to hold the seven samples.

(3) Seven drivers and seven resistors connected to a Schmitt trigger (voltage comparator) to add the samples and decide if the majority are 1's or 0's; the Schmitt trigger output conditions the main shift register.

(4) Two digital comparators, (A) to compare flip-flop 1 with flip-flop 7, and (B) to compare flip-flop 1 with the output of the Schmitt trigger.

(5) A 3-bit counter (J–K flip-flops 8, 9, and 10) capable of being gated to count by 6, 7, or 8 by using its own output pulse to reset its second or first flip-flops. For a count of 8, none of the flip-flops are reset. The output pulse is also used to load the output of the Schmitt trigger into the main shift register and to shift the latter.

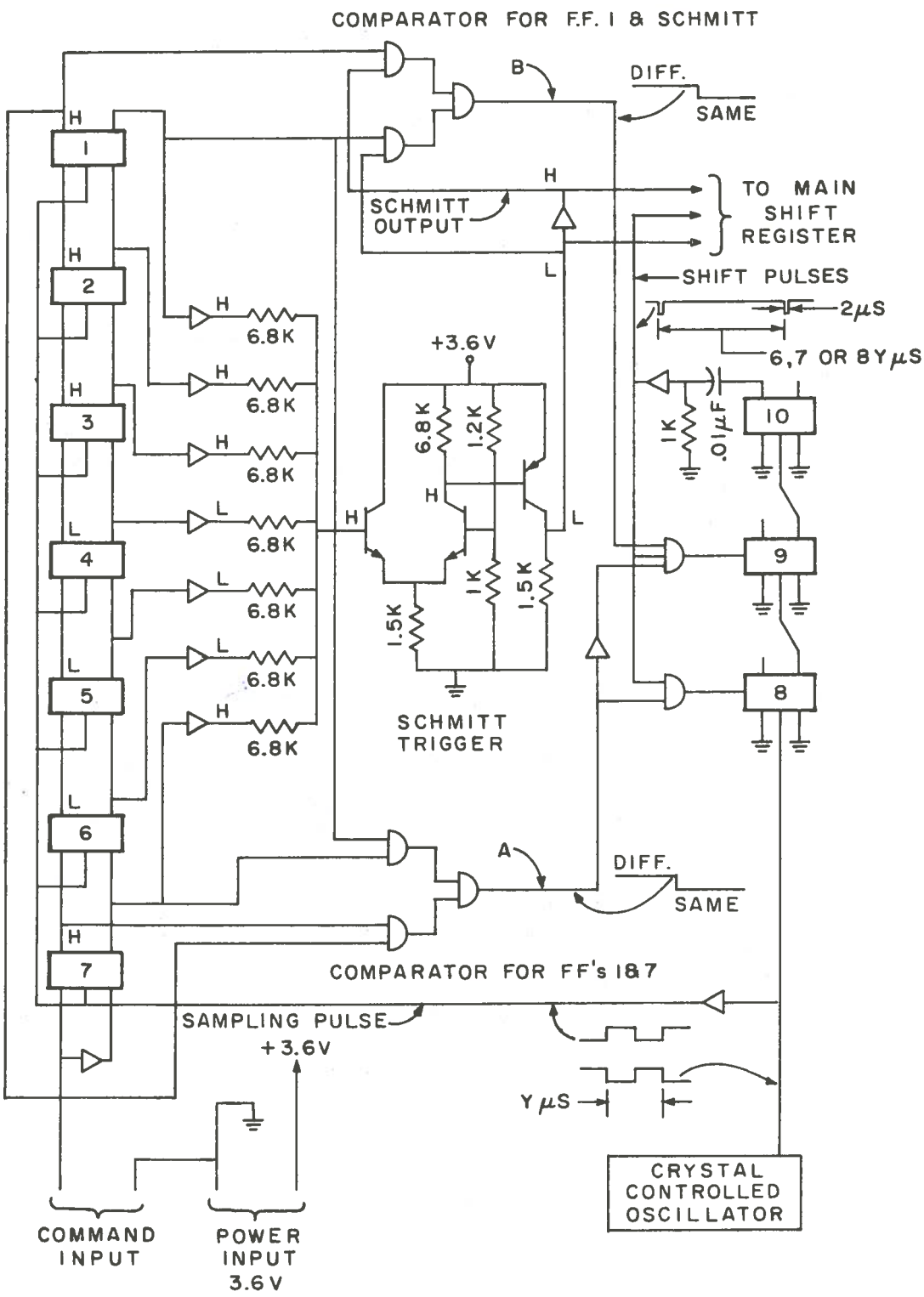


Figure 7 Bit-timing recovery – circuit diagram

When proper bit-timing has been achieved, the counter will divide by 7. The output pulse will be advanced by one sample (1/7 bit-time) if the counter divides by 6, and it will be retarded by one sample if the counter divides by 8. Bit-timing is correct if the output pulse from the counter occurs when all the samples in the sample register are of the same bit. Bit-timing is incorrect if the output pulse occurs when some of the samples are of a bit before a transition in the data waveform, and the rest of the samples are of a bit after the same transition. The output pulse will be *advanced* or *retarded* depending on which will achieve correct bit-timing faster. A maximum of three transitions in the data is required to reach correct bit-timing.

Table I shows the eight possible combinations of flip-flops 1 and 7 and of the Schmitt output. The corresponding outputs of the comparators and their effect on the counter are also shown.

Table I

Samples			Comparators			Meaning
F.F.1	F.F.7	Schmitt	F.F.1 & F.F.7 A	F.F.1 & Schmitt B	Counter will divide by	Next shift pulse will be in
0	0	0	low	low	7	1 bit-time
0	0	1	low	high	7	1 bit-time
0	1	0	high	low	6	6/7 bit-time
0	1	1	high	high	8	1-1/7 bit-time
1	0	0	high	high	8	1-1/7 bit-time
1	0	1	high	low	6	6/7 bit-time
1	1	0	low	high	7	1 bit-time
1	1	1	low	low	7	1 bit-time

Referring to Table I and the circuit diagram we can see the following:

(a) When flip-flops 1 and 7 are the same, A is low and the counter divides by 7 because the 2-μsec output pulse is allowed to reset flip-flop 8 and not flip-flop 9.

(b) When flip-flops 1 and 7 are different, A is high and flip-flop 8 will not be reset, but if flip-flop 1 and the Schmitt are the same, flip-flop 9 will be reset (because B is now low). The counter then divides by 6.

(c) If flip-flops 1 and 7 are different and flip-flop 1 and the Schmitt are also different, then both A and B are high and none of the flip-flops will be reset. The counter then divides by 8.

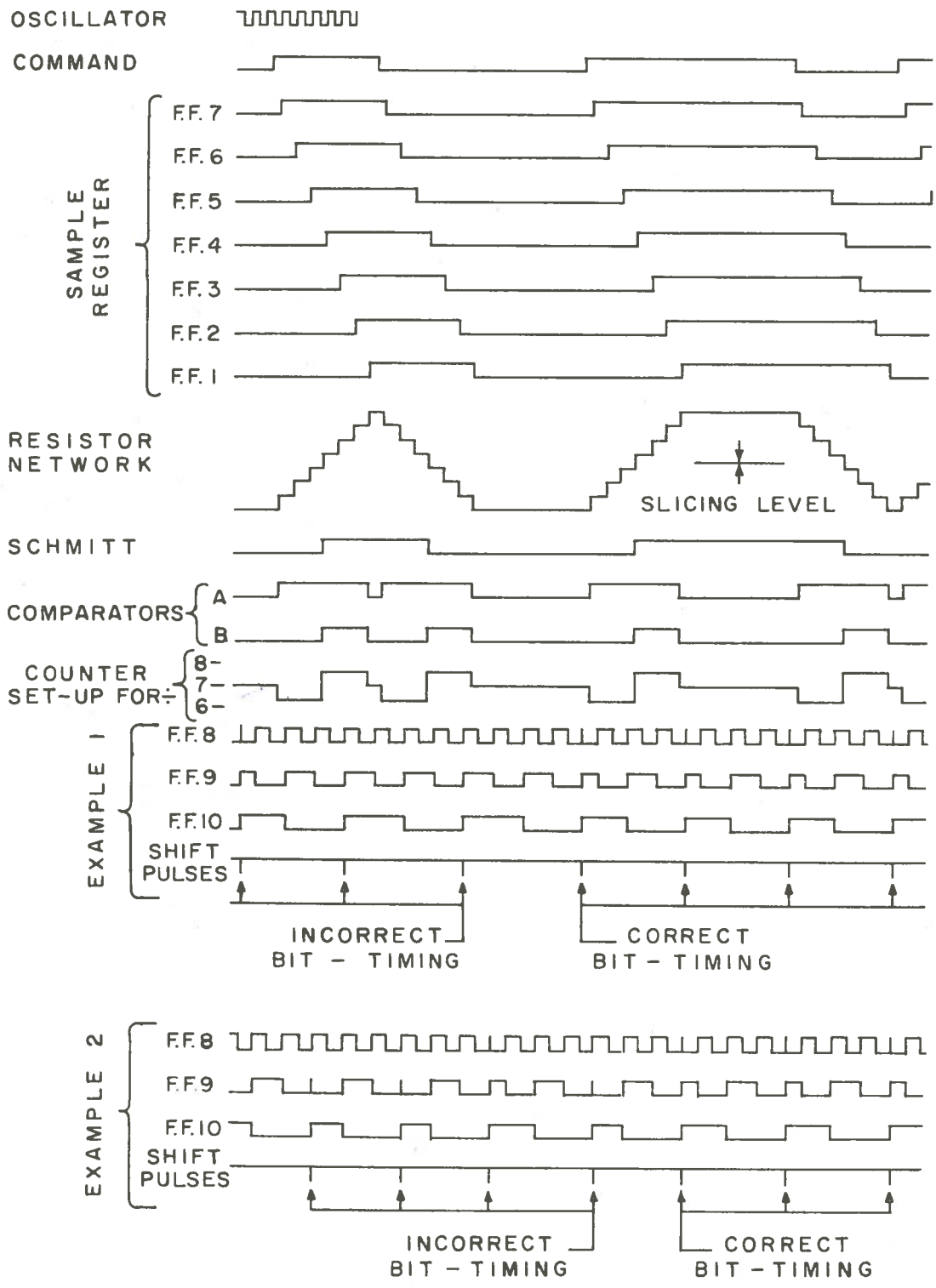


Figure 8 Bit-timing recovery – waveforms

If correct bit-timing is disturbed by a noise pulse it will be restored at the next data transition. This will not prevent the main shift register from being loaded properly. In fact, the bit-timing could be out by as much as ±3 samples (3/7 of the bit-time) and the main shift register would still be loaded properly, provided that four *consecutive* samples were correct and of the same bit. When bit-timing is correct any four good samples will allow proper loading of the main shift register. Example 1 in Fig. 8 shows how correct bit-timing is achieved by retarding the shift pulses. Example 2 shows how correct bit-timing is achieved by advancing the shift pulses.

Logic Circuitry and Decoding

The circuit diagram and waveforms are shown in Figs. 9 and 10, respectively. The command bit stream at the output of the Schmitt trigger is shifted into the main shift register. This register has nine flip-flops and the first is compared with the last.

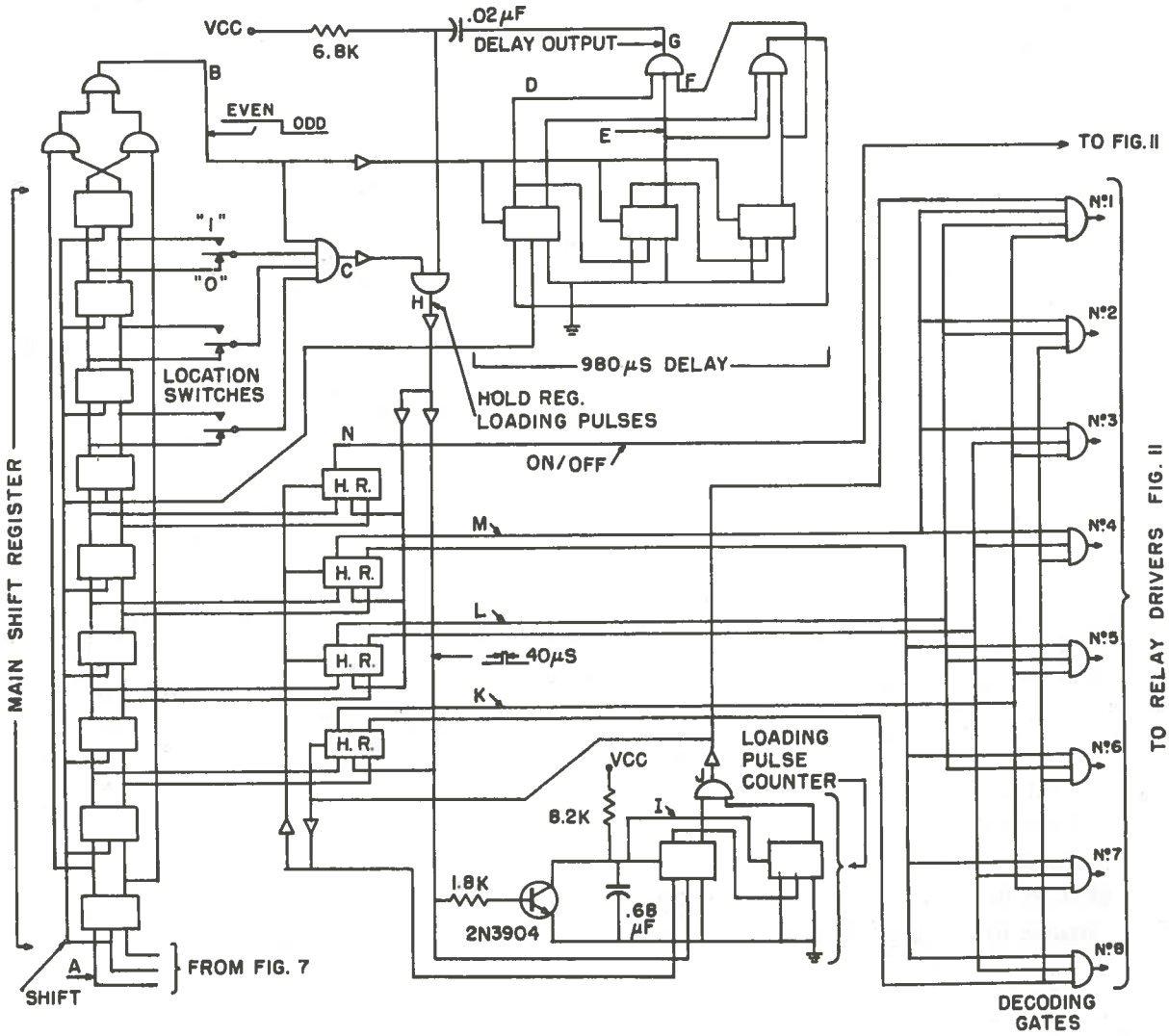


Figure 9 Logic circuitry and decoding

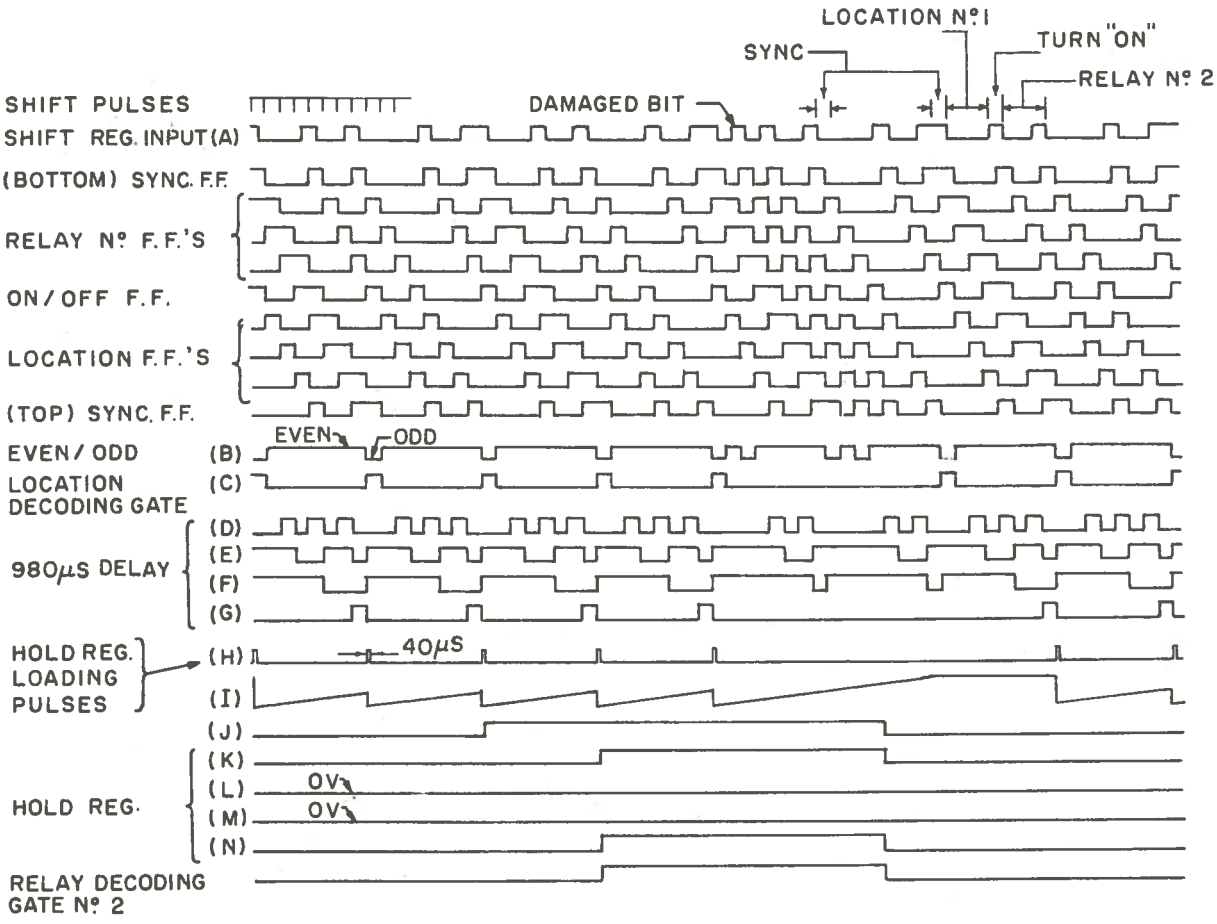


Figure 10 Logic circuitry – waveforms

With this arrangement, all the bits of one word are compared with the corresponding bits of the next word. The comparator (B) produces a high level when corresponding bits are the same, and a low level when they are different (like 2 sync bits). The transition from a low to a high level initiates a counter type delay, the counter having been reset by the low level. The delay (G) will produce one 40-μsec pulse after counting for 980 μsec, provided that the delay is not reset by the comparator during that 980 μsec. This pulse will coincide with the next low level of the comparator. Thus a 40-μsec pulse will be produced at (H) by ANDing the comparator low level, the delayed pulse, and the three location bits. This is a conditional loading pulse for the hold register and it will be produced *only* if at least two successive words plus the sync bit of the third word are correct (undamaged by noise). Furthermore, the loading pulses are counted and four consecutive pulses are required before the hold register will actually be loaded with the command bits, on the trailing edge of the fourth pulse. These bits will be held until one or more loading pulses are missed. In this event, the hold register will return to all 0's until another four consecutive loading pulses are produced.

The bottom 3 bits of the hold register are decoded by 8 gates. The outputs of these gates plus the ON/OFF bit (top flip-flop of the hold register) turn 8 latching relays ON or OFF. The output J of the loading pulse counter also prevents decoding gate No. 1 from being enabled when the hold register is all 0's because of the absence of loading pulses.

Relays and Relay Drivers

The unit contains 8 latching relays each having 2 windings. One to turn the relay ON and one to turn it OFF. Figure 11 shows the circuit diagram. The top ends of all the 'turn on' windings are connected together and will be held at +12 volts by a relay driver transistor if the ON/OFF flip-flop (top flip-flop in the hold register) is in the 1 state (left collector is high). The top ends of all the 'turn off' windings are connected together and will be held at +12 volts if the ON/OFF flip-flop is in the 0 state.

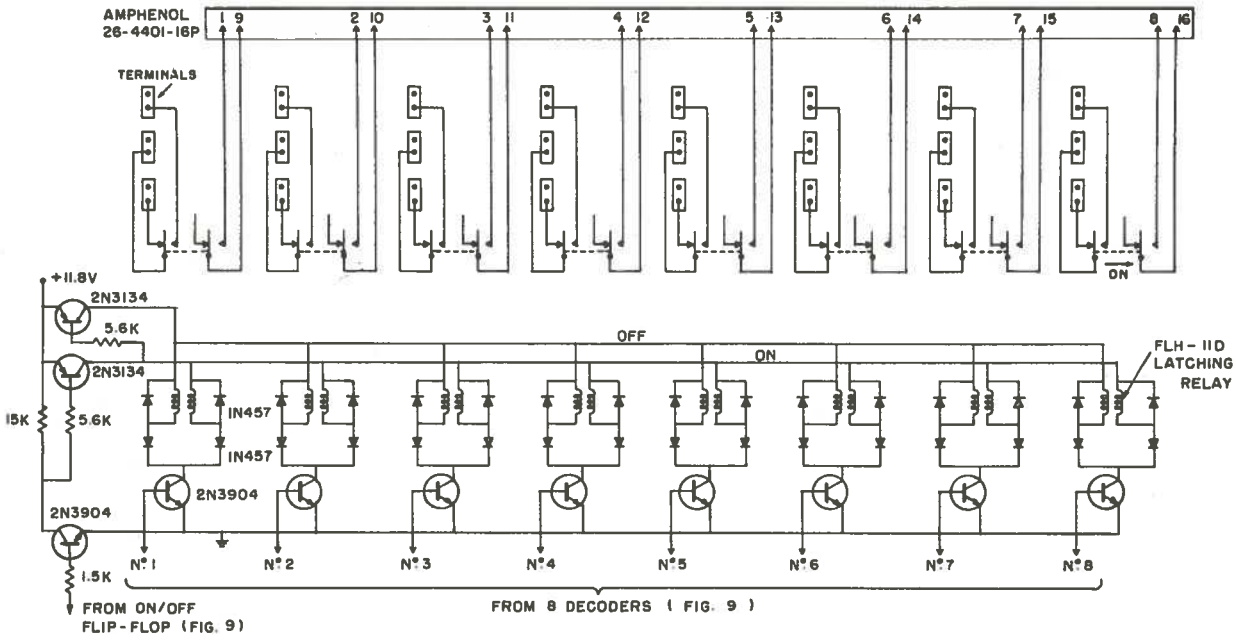


Figure 11 Relays and relay drivers

If a decoding gate is enabled, the bottom ends of both windings of the associated relay will be held at ground level by a relay driver transistor and the relay will be forced to the ON state if the ON/OFF flip-flop is in the 1 state. The relay would be forced to the OFF state if the flip-flop was in the 0 state.

Diodes are connected in series with each winding to prevent unwanted current flow from the turn on line to the turn off line. The diodes across each winding prevent voltage spikes, which could damage the transistors.

Testing

A solid state programmer was built and used to produce automatically the 16 possible commands for one location. Each command is transmitted for one second with an

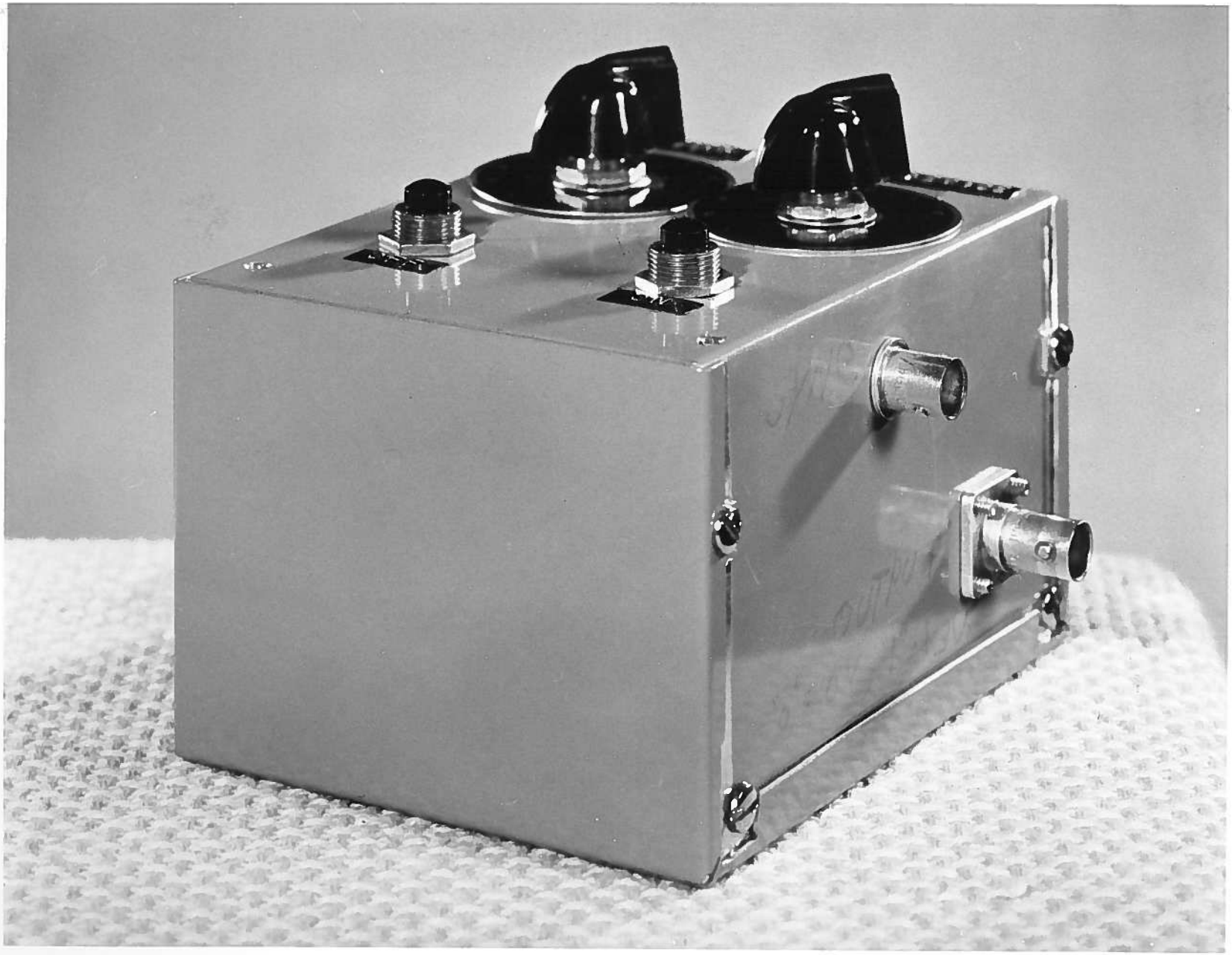
interval of one second between commands. During this interval the idling pattern is transmitted in order to keep the power on between commands. After all the 16 commands are transmitted, the transmitter is turned off. Thus about every five minutes the transmitter is turned on for 32 seconds and the set of 16 commands is transmitted. A multipen recorder at the receiving end shows the operation of the 8 relays.

Conclusion

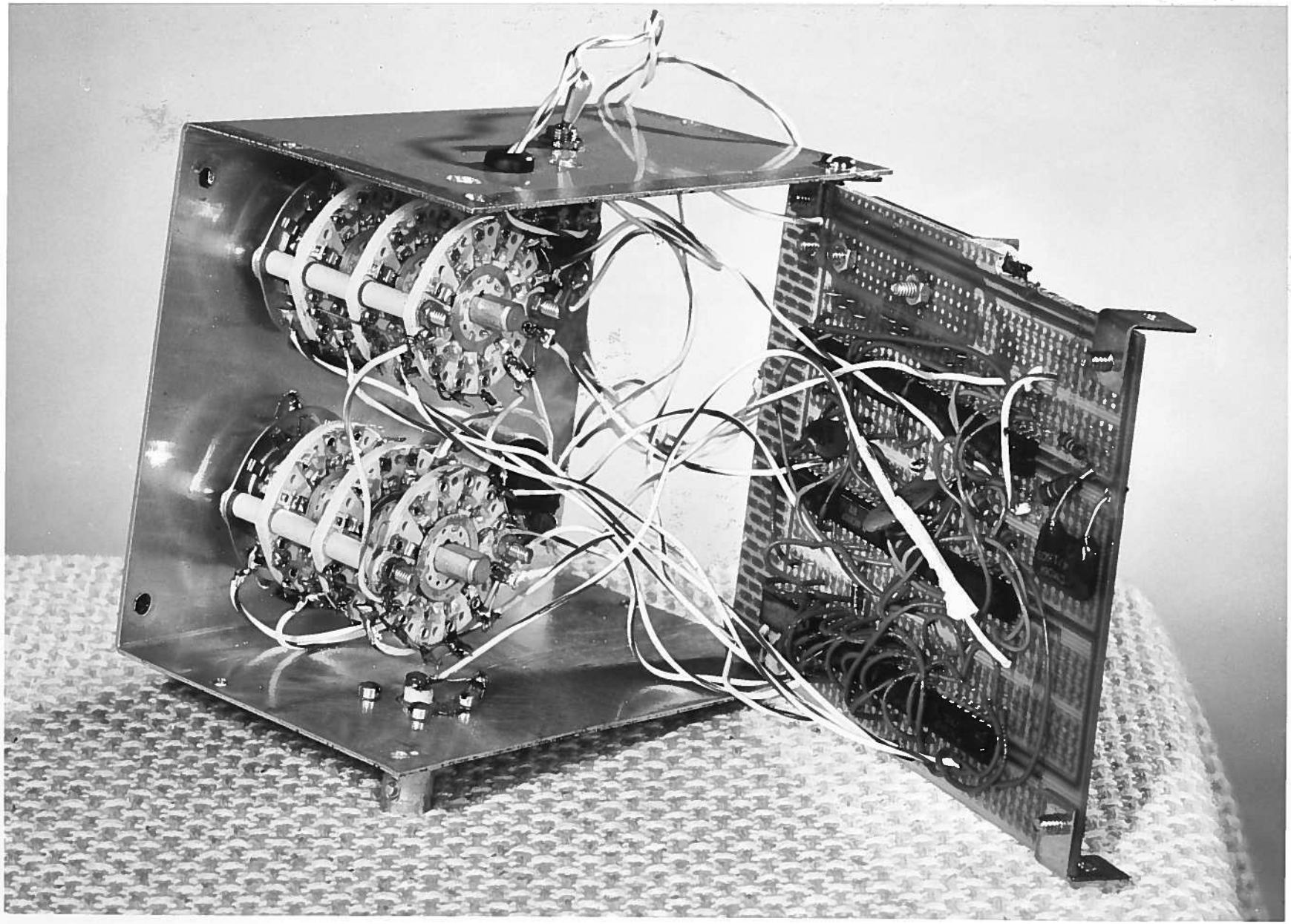
The tests over a radio link have been very encouraging. Reliable performance with no false operations has been achieved, even in the presence of appreciable noise pulses from other radio signals. Although designed with lighthouse control in mind, this system could be used for any other application where a limited number of ON/OFF functions are required.

Acknowledgments

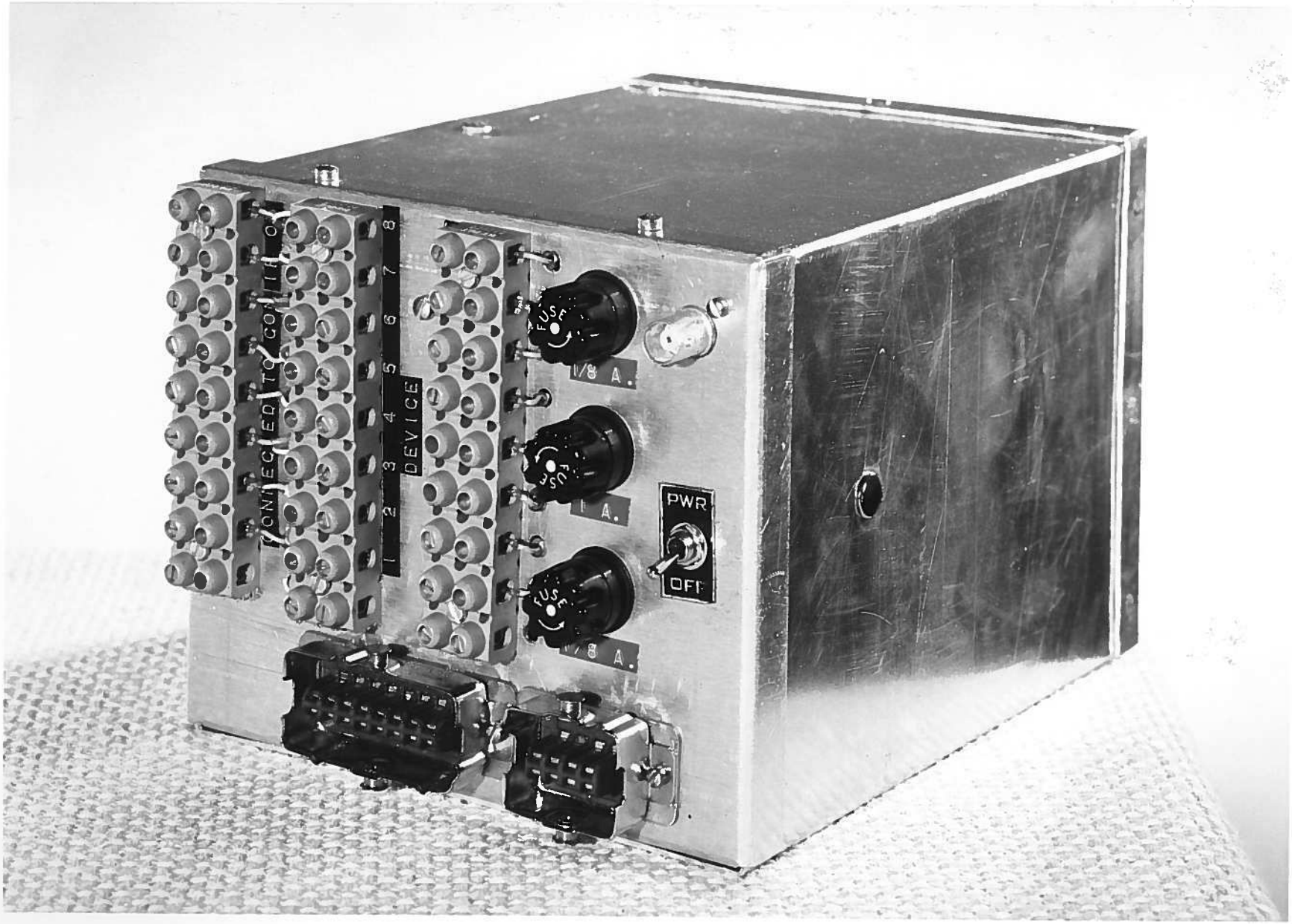
The author wishes to acknowledge the assistance and suggestions received from other members of the Navigational Aids Section, especially with setting up the radio links.



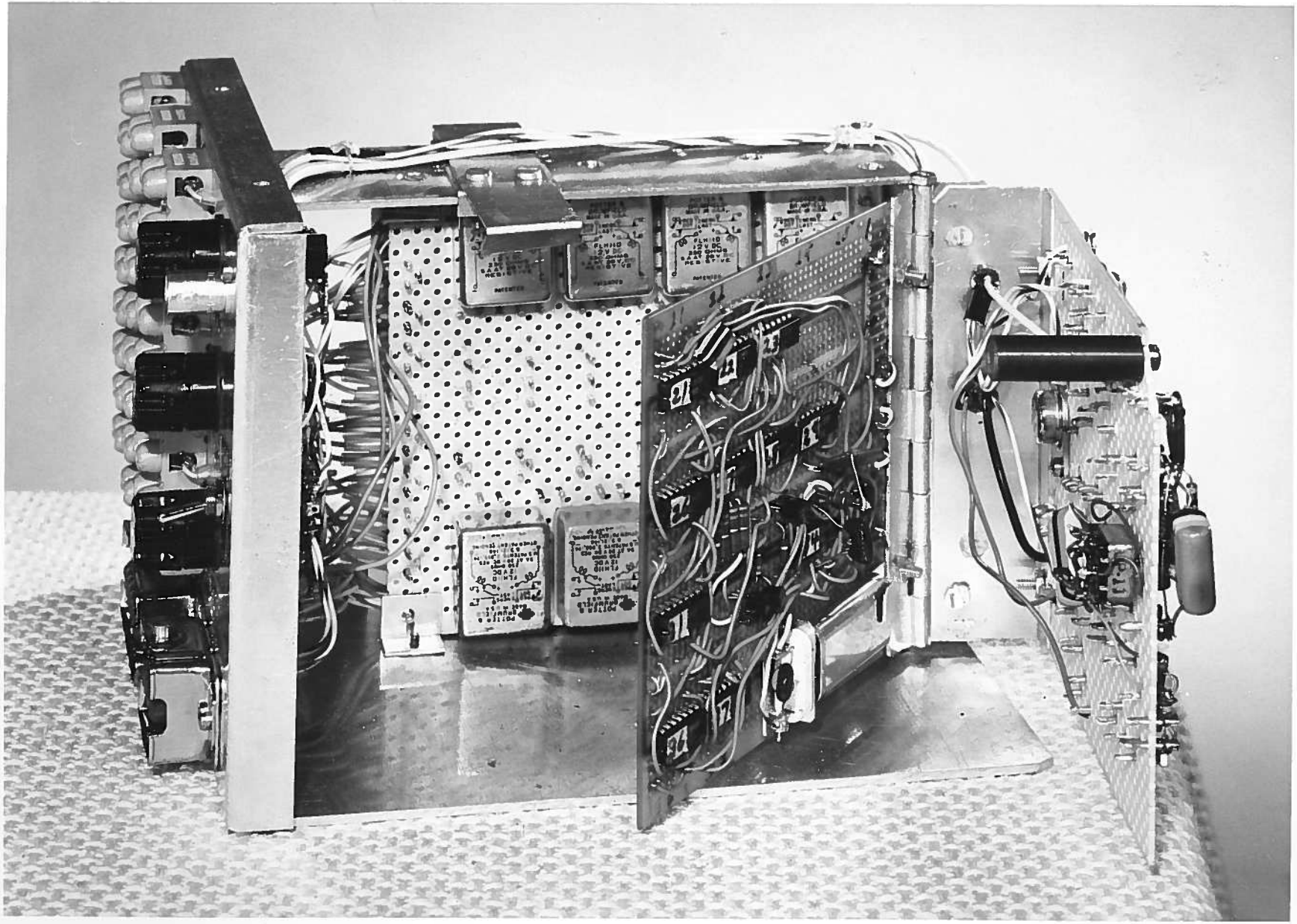
Photograph #1 - Logic Circuitry - transmitting end.



Photograph #2 - Logic Circuitry - transmitting end



Photograph #3 - Logic Circuitry - receiving end



Photograph #4 - Logic Circuitry - receiving end