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Vertically tapered waveguide spot size converters fabricated via a linewidth controlled grey tone lithography for InP-based photonic integrated circuits

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Abstract: We report a novel and simple fabrication process to realize vertically tapered spot size converters (SSC) on InP photonic integrated circuits. The vertical tapering was achieved via a linewidth controlled local optical dose variation, leading to a grey tone photoresist profile. The fabricated SSCs are compact, polarization insensitive and demonstrate a very high mode conversion efficiency of 95%. Integrated SSCs improved the overall loss by 5 dB giving a coupling loss as low as 1.3 dB/facet, for a lensed fibre with a mode field diameter of 3.0 µm. A good agreement was found between the fibre-to-fibre optical loss measurements and those predicted from simulations.

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1. Introduction

The indium Phosphide (InP) material system has a very strong potential to enable the integration of various active and passive optoelectronic components on a single substrate. This allows the cost-efficient manufacturing of compact photonic integrated circuits to efficiently generate, manipulate and detect optical signals. However, InP photonic devices suffer from a larger chip to fiber coupling losses compared to other material systems [1]. On-chip photonic waveguides (WGs) in semiconductor platforms such as InP/InGaAsP and silicon typically support a non-circular mode with an optical mode field diameter (MFD) on the order of 1 µm, while commercial optical fibres have a circular mode and a much larger MFD approaching 10 µm across. This mode size mismatch results in a large optical coupling loss between an optical fibre and a photonic chip [2,3]. The coupling loss can be reduced by using special fibres and micro-optic components, but this requires a costly packaging process [4]. Therefore, it is essential to monolithically integrate a spot size converter (SSC) at the input and output ends of a photonic chip to reduce the fibre to chip coupling losses [5–12].

Among the various SSC fabrication technologies used in the InP/InGaAsP platform, vertical coupling and butt-joint (BJ) coupling are commonly practiced. In the vertical coupling method, the lateral tapering of the WG width is used to expand the mode in the vertical direction forcing the light to couple into a second underlying low index contrast WG with a much larger MFD. Low index contrast waveguides are easily created using dilute InGaAsP/InP alloys [10,11]. This approach is effective where the primary high index waveguide core thickness is below 0.5 µm, and offers a very large fibre misalignment tolerance. However, it requires a very tight control over the width and profile of the primary WG taper. In the BJ coupling method, vertical tapering of the core thickness and lateral expansion of the WG width are used to increase the mode size in deep ridge WGs [7,9]. The vertical tapering of the core thickness is typically achieved via a selective area growth (SAG) technique [7,12], grey-tone lithography [13] or a micro-loading

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technique [9]. In the SAG method, first the wafer is patterned and the primary WG is completely etched off near the coupling facet. Then the SAG technique is used to overgrow a new WG core in the etched regions. By growing through a masked aperture of varying width, the effect of loading on growth rate can be used to control WG core thickness. The SAG mask pattern is tapered to produce a thicker core (high mask loading) at the junction between the original primary WG and the newly grown WG, and a gradually thinner core toward the cleave facet (low mask loading). This method is very robust in terms of the control over the SSC profile and the core thickness at the cleave channel. However there is a WG discontinuity at the butt junction which could create back-reflections and mode mismatch loss. Minimizing these effects requires a tight control over the alignment and composition of the SSC core. Furthermore, it requires a complex and lengthy process. In the grey-tone method, the wafer is patterned using a grey-tone mask with arrays of holes smaller than the lithographic resolution to form a 3D profile in the photoresist [13]. Then the photoresist profile is either transferred directly to the semiconductor underneath via a dry etch process, or first to an underlying dielectric and then to the semiconductor underneath. The main issue with the grey-tone method is the process repeatability and the complexity of the mask design. In the micro-loading method, the dependence of dry etch rate on the mask loading is utilized to form a vertically tapered core after the etch process. This method offers a very simple fabrication process, however the taper length is limited to below 20 µm [9], and therefore the fabricated SSCs are not sufficiently adiabatic and can suffer from back reflections and losses.

In this work, we are introducing a novel method to fabricate vertically tapered SSCs using a very simple, versatile and manufacturable method based on the manipulation of the image focal plane during optical mask exposure. The results of fibre-to-fibre loss measurements will be presented, and will be compared to the predictions from simulations.

2. Design and fabrication and loss measurement setup

The epitaxial growth was carried out on 3” InP substrates using a multi-wafer vertical closed coupled shower head metalorganic vapor phase epitaxy (MOVPE) reactor. The first growth consisted of an InP underclad, and an InGaAsP-based multi-quantum well (MQW) stack with a total thickness of 550 nm to form the primary WG core, and an InP overcladding layer with a thickness of 100 nm. The investigated MQW has a photoluminescence emission wavelength of ~ 1400 nm and is commonly used in the production of Mach-Zehnder modulators [7]. The grey region in Fig. 1(a) shows the etch mask design for an SSC with two sequential laterally tapered segments connecting the primary WG with a non-tapered segment at the facet. The laterally tapered segment(s) is where the WG MQW core thickness will be vertically tapered, and the non-tapered segment is where the device will be cleaved to form the input/output coupling facets at the both ends of the device. After spin coating the wafers with 5 µm of an OiR908-17 photoresist, the wafers were patterned using an ASML 5X i-line stepper. A negative focus offset of 5 µm during the photoresist exposure, with a dose of 400 mj/cm^2, results in a local optical intensity modulation that is proportional to the lateral linewidth of the mask features. A zero focus offset is where the laser beam is focussed on the top surface of the photoresist. To apply a negative focus offset, the stepper stage moves up toward the photomask from the zero focus offset position. Mask features narrower than the defocussed optical resolution limit will produce a lower optical exposure dose at the photoresist layer, while wider features will still receive the full optical intensity across most of their cross-section. The solubility of the photoresist in a developer is proportional to the exposure dose. Developing the photoresist, using an OPD-4262 developer, results in a vertical tapering of the photoresist thickness along the laterally tapered segments, with the photoresist thickness decreasing from the BJ toward the cleave channel. At the end of this process, the grey region in Fig. 1(a) remained covered with photoresist, and the photoresist was completely removed in the cleave channel. After a flood deep ultra-violet (DUV) exposure treatment, to harden the photoresist, the wafers were dry etched in a surface technology systems

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(STS) inductively coupled plasma (ICP) etcher at room temperature using a $Cl_2/Ar/N_2$ chemistry. To effectively translate the photoresist thickness profile to the semiconductor underneath, one must balance the semiconductor etch rate relative to the photoresist etch rate. For a given ICP source power, increasing the platen power and Cl_2 flow rate increases the etch rates of both the semiconductor and the photoresist. However, we found that the photoresist erosion rate increases more dramatically with increasing the platen powers and Cl_2 flow rate, leading to a reduced SSC taper length. N_2 and Ar were used to dilute Cl_2 and to promote the plasma ignition and stability. Optimum etch condition resulted in a low InP/InGaAsP etch rate of ~ 0.1 µm/min and was obtained by setting the ICP source voltage to 500 V, platen power to 30 W, $Cl_2/Ar/N_2$ flows to 5/10/40 sccm and working pressure to 10 mTorr. Representative examples of the etched profiles, measured by a profilometer, are shown in Fig. 1(b). The length of the vertically tapered section was ~ 10% shorter than the layout length of the laterally tapered segment(s). After removing the remaining photoresist, via a combination of O_2 plasma and wet solvent etching, and a preclean process using phosphoric and hydrofluoric acids, a thick undoped InP overclad was grown in the MOVPE reactor. Subsequently, one micron oxide was deposited and patterned using an OiR 620 photoresist. After etching the oxide mask and stripping the photoresist, the WGs were formed by etching the wafers using an HBr-based chemistry in an STS ICP etcher at an elevated temperature of 180 °C. The ridge WG width was linearly increased from the BJ toward the end of the SSC taper to laterally expand the mode size, as shown schematically in Fig. 1(a). Finally, after deposition of a dielectric cladding layer, the wafers were thinned down to 250 µm thickness, cleaved and both facets were anti-reflection (AR) coated. The facet coating stack consisted of alternating layers of SiO_2 and TiO_2, deposited using a plasma enhanced chemical vapor deposition technique. A 3D representation of a fabricated SSC is shown in Fig. 1(c).

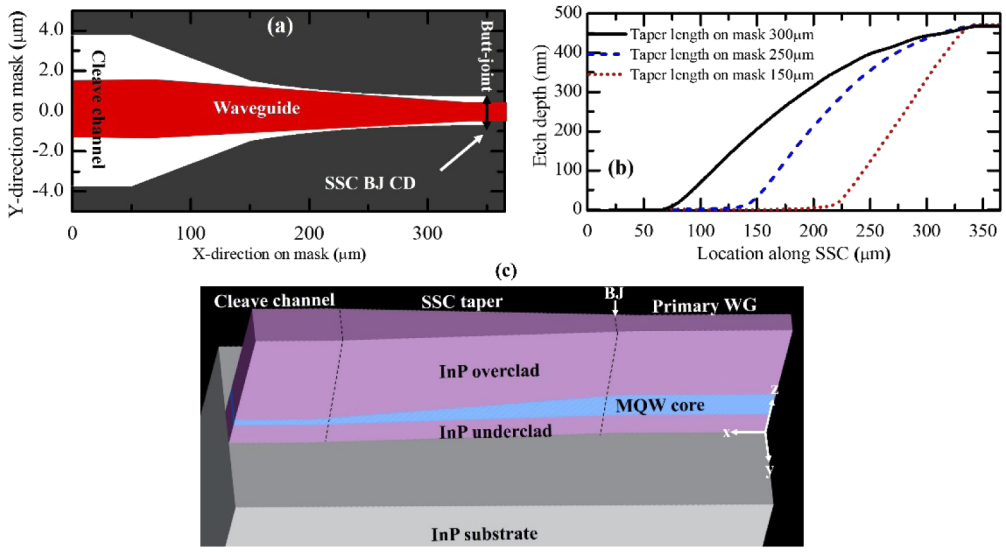

Fig. 1. a) Schematic of the SSC layout (grey color) with two laterally tapered segments and a non-tapered cleave channel, and the waveguide layout (red color). b) Representative fabricated, and measured, vertical profile of SSCs with three different taper lengths and design after a dry etch step. c) A 3D representation of a fabricated SSC.

SSC layout design parameters included the taper shape, taper length, and the layout linewidth at the BJ. Hereinafter, the layout line width at the BJ will be referred as SSC BJ critical dimension (CD), as shown in Fig. 1(a). Several lateral layout taper shapes were fabricated and assessed: a single segment exponential taper (E), a single segment linear taper (L), a two segment linear

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taper (LL), a two segment linear-exponential taper (LE), and a two segment exponential-linear taper (EL). The length of the tapered segments was in the range of 100 µm to 400 µm. The SSC BJ CD was in the range of 2.5 µm to 5.0 µm. The core thickness at the coupling facets was ~ 90 nm or ~ 120 nm. All the results presented here are from devices with a facet core thickness of ~ 120 nm, unless otherwise mentioned. The length of the primary WG was 1cm, and each cleaved bar contained 30 devices.

The total fibre-to-fibre optical insertion loss was measured by launching light into and out of the chip using polarization maintaining single mode spherical lensed fibres with a 3.0 µm MFD at the facet. The input and output fibres were simultaneously coupled to the input and output WG facets using a piezoelectric computer-controlled stage. The output signal was acquired while scanning the input laser wavelength with a step of 0.1 nm from 1545 nm to 1555 nm. After removing the system loss, the measured insertion loss was taken as the integrated average over this spectral range. The measurements were carried out using both TE- and TM-polarized signals. To reduce the measurement noise, from the scattered light, the input and output WG facets were designed to have a lateral offset of 300 µm by including two bends with radii of 150 µm in the middle of the straight WGs.

3. Results and discussion

A low loss SSC requires a smooth and gradual tapering of the core thickness through the BJ region. We found that, under the process conditions established in this work, the SSC BJ CD must be below 3.5 µm to provide a smooth transition at the BJ, with the core thickness reducing gradually without forming an abrupt step at the BJ. Representative scanning electron microscope (SEM) images from a device with an SSC BJ CD of 3.0 µm and 4.0 µm are shown in Fig. 2(a) and (b), respectively. The device with a larger SSC BJ CD shows an abrupt decrease of the core thickness at the BJ, and is expected to cause an excess scattering loss. For larger SSC BJ CDs, the photoresist thickness at the BJ is thinner and therefore the photoresist is completely eroded

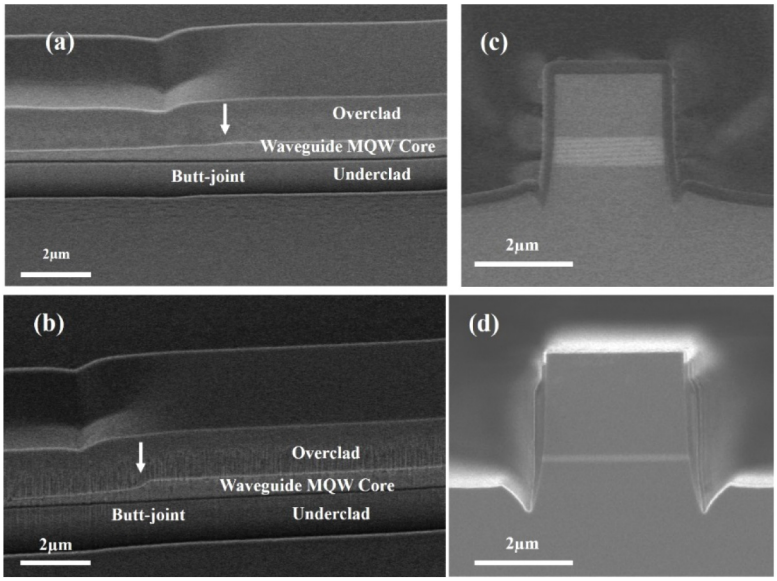

Fig. 2. SEM images from the BJ regions of a fabricated device with an SSC BJ CD of (a) 3.0 µm and (b) 4.0 µm. SEM cross-section images from WG (c) outside SSC and (d) at the cleaved coupling facet.

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before the etch has reached the desired depth at the cleave channel, resulting in the formation of a step at the BJ. Cross-section SEM images from a fully processed device perpendicular to the WG outside the SSC (primary WG) and the output coupling facet are shown in Figs. 2(c) and (d), respectively. The MQW core thickness (lateral WG width) was 550 nm (2.1 ± 0.1 µm) outside the SSC and 120 nm (3.1 ± 0.1 µm) at the facet. One standard deviation of the cross wafer and wafer to wafer variation of the core thickness at the coupling facet was 8 nm.

Figure 3 shows a box plot of the fibre-to-fibre loss measurements of over 200 devices with various SSC design parameters, as well as the loss measured for reference WGs without integrated input/output SSCs. It is clear that the integrated SSCs with optimum design are effective in reducing the coupling loss by ~ 5 dB.The data suggests that the SSC layout taper shape does not have a significant impact on the SSC performance. Furthermore, the SSCs perform equally well for both TE- and TM-polarized signals.

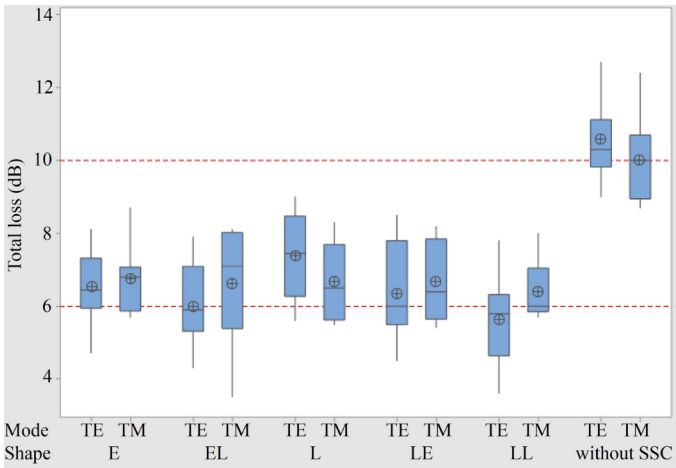

Fig. 3. Boxplot of the measured fibre-to-fibre optical loss of the reference WGs and the SSCs with various designs for TE- and TM-polarized signals. The circles inside the boxes represent the mean value of the measured losses. The dashed horizontal lines are guides to the eye.

The SSC BJ CD and the SSC taper length were found to be the main factors impacting the SSC performance, as shown in Fig. 4. The best SSC performance was obtained for SSC taper lengths below 120 µm, and SSC BJ CD of less than 3.5 µm. The observed trend of the elevated loss with increasing the SSC BJ CD is consistent with our observation of the BJ WG discontinuity in Figs. 2(a) and (b). The devices with a larger SSC BJ CD had an abrupt decrease of the core thickness at the BJ. In the extreme case, the core thickness abruptly changed from 550 nm to ~ 120 nm at the BJ which is expected to result in a large mode mismatch loss and back-reflections. In practice, the SSC taper length must be sufficiently long to ensure a smooth adiabatic mode conversion. However, the scattering loss caused by sidewall roughness/defects is larger for longer SSCs. Our results in Fig. 4 shows that the shorter SSCs perform better suggesting that the mode conversion loss is smaller than the defect related scattering losses at the SSC region.

To further evaluate the optical loss contributions, we fabricated and tested two groups of devices. The first group consisted of WGs with various lengths with no integrated SSCs at the input and output facets. For this group, the optical losses may originate from the fibre-to-chip coupling losses and WG propagation loss caused by scattering from sidewall roughness/defects. From the linear fits to the fibre-to-fibre loss measurements of this group, shown in Fig. 5(a), a WG propagation loss of 0.9 ± 0.4 dB/cm and 1.1 ± 0.4 dB/cm were obtained for TE- and TM-polarized launch signals, respectively. These measurements are consistent with the commonly reported

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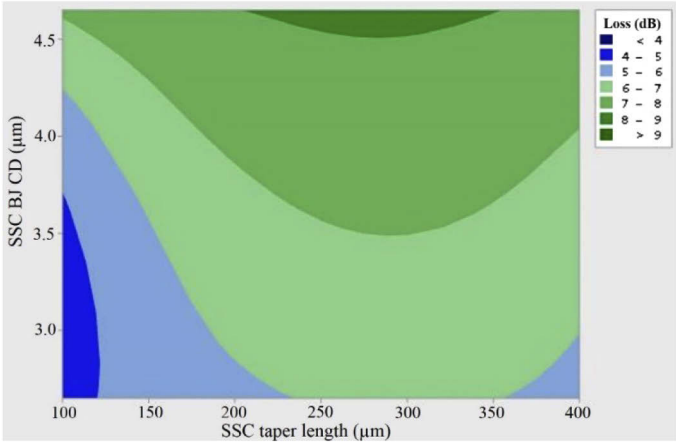

Fig. 4. Contour plot of the measured fibre-to-fibre optical loss as a function of SSC BJ CD and total SSC taper length.

WG propagation loss values [1], but somewhat larger than those reported for undoped buried ridge InGaAsP/InP WGs with a ~ 500 nm bulk quiding layers emitting at a photoluminescence wavelength of 1250 nm [14]. The second group included the reference WGs with input/out SSCs, and two other structures with two or four additional SSCs integrated along the WG back to back in series. A schematic of a test structure with six SSCs is shown in Fig. 5(b). All SSCs had an identical design with an SSC BJ CD of 3.5 μm and a taper length of 300 μm. The results shown in Fig. 5(c) gives an SSC propagation loss of 0.2 ± 0.1 dB/SSC for both TE- and TM-polarized launch signals. This translates to 95% mode conversion efficiency of the fabricated SSCs. The

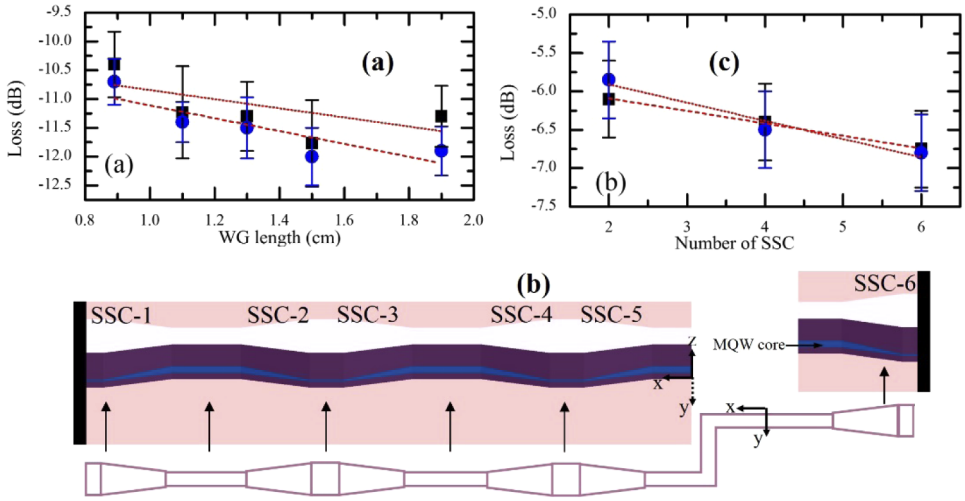

Fig. 5. Plot of the measured fibre-to-fibre optical loss of a) the reference WGs without integrated SSCs as a function of their length, and c) the WGs with various numbers of integrated back to back SSCs. b) a schematic of a test structure with six integrated SSCs. Black squares and blue circles correspond to the TE- and TM-polarized launch signal, respectively. The dotted and dashed lines are the linear least square fits to the data. Each data point represents the mean of the measurements on 8 different devices, and the error bars represent one standard deviation of the measured loss values.

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SSC propagation loss may originate from the scattering at the sidewalls and the regrowth interface between the InP overclad and the etched InGaAsP MQW core along the SSC WG. Also, the scattering at the transitions points, i. e. transition at the BJ and the transition at the end of the tapered segment and the cleave channel, may contribute to the SSC propagation loss. From the data presented in Figs. 3 and 4, the fibre-to-fibre loss of the devices with the optimum input/output SSC design parameters was in the range of 4.0 dB to 5.0 dB. From the data presented in Fig. 5, the primary WG and SSC propagation losses account for ~1.4 dB, and therefore an estimate of the fibre to SSC coupling loss was in the range of 1.3 dB to 1.8 dB per facet. This translates to 65% to 75% coupling efficiency per facet for the designed and fabricated SSCs. Depending on the design of the primary WG and SSC, the complexity of the SSC fabrication process and the MFD of the coupling fibers, the SSC loss in an InP platform is typically in the range of 1 dB to 2 dB [1,5,6,9,15–18]. Despite the ultra compact design of our fabricated SSCs (~ 100µm SSC length) and the simplicity of our fabrication process, our measured SSC losses compare well with those reported previously.

In the following, we will compare these experimental results to the predictions from simulations. Lumerical's commercial 2D finite domain eigenmode (FDE) and 3D eigenmode expansion (EME) methods were used to calculate the fibre to chip coupling loss and the SSC propagation loss, respectively, at a wavelength of 1550 nm. Based on EME calculation, using near optimum design parameters, the SSC shape had a negligible impact on the SSC propagation loss. However, a reflection was predicted for SSCs with a taper length less than 50 µm.

Figure 6(a) shows the side view refractive index profile along an SSC with a linear taper of the MQW core thickness. The corresponding fundamental TE mode field profile shows a clear mode expansion as the MQW core thickness decreases toward the facet, as shown in Fig. 6(b). Figures 6(c) and (d) show the refractive index profiles of the WG cross-sections outside the SSC and at the coupling facet, respectively. The effective refractive index of the fundamental TE mode at the BJ and the coupling facet are 3.30 and 3.19, respectively. The mode field size increases from 1.4 µm × 1.9 µm outside the SSC in the primary WG to 3.0 µm × 2.8 µm at the coupling

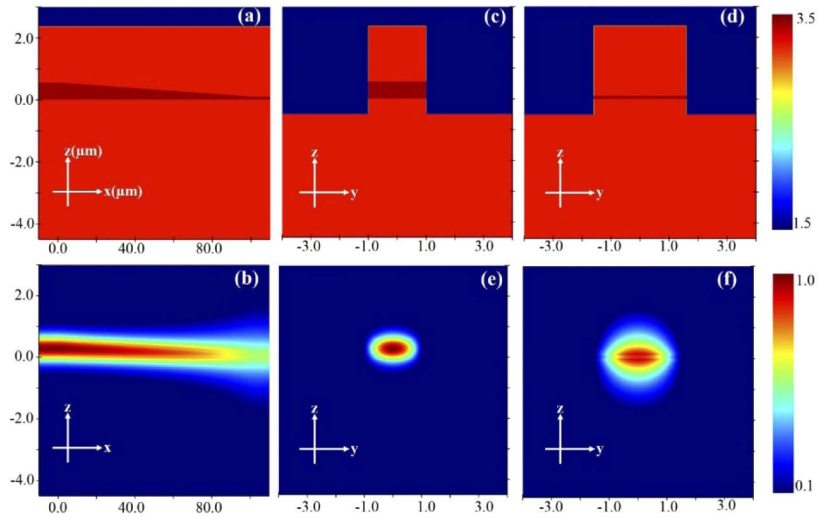

Fig. 6. a) Side view refractive index profile along an SSC and b) the corresponding fundamental TE mode field profile. Refractive index profiles of the WG cross-sections c) in the primary WG before the the SSC and d) after the SSC at the coupling facet, and the corresponding simulated TE mode field profile in (e) and (f), respectively. The core thickness at facet was 110 nm.

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facet, as shown in Figs. 6(e) and (f), respectively. The increase of the facet mode size in the lateral (vertical) direction is the result of increasing (decreasing) the WG width (core thickness). The calculated SSC propagation loss, shown in Fig. 7, slightly improves with increasing the SSC taper length and reducing the WG width gradient along the SSC, consistent with a more adiabatic mode conversion along the SSC. Within the experimental parameters ranges, the calculated SSC propagation loss only contributes 0.1 - 0.2 dB to the total loss, consistent with our measured value of 0.2 ± 0.1 dB. For an SSC with a taper length of 100 µm, the propagation loss is negligible for facet core thicknesses above 150 nm, as shown in Fig. 8. As the facet core thickness decreases below 150 nm, the vertical taper rate increases leading to elevated propagation losses. For these calculations, a smooth BJ transition was assumed.

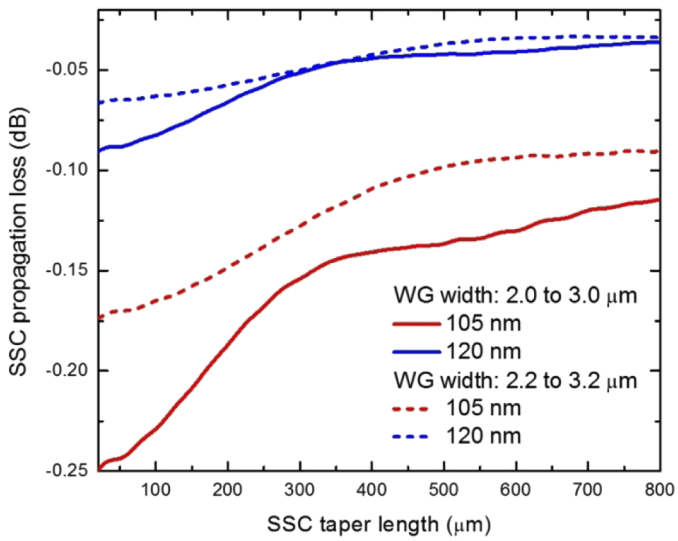

Fig. 7. Plot of the calculated SSC propagation loss for TE mode as a function of the SSC taper length for two different facet core thicknesses. The WG width was linearly varied from 2.0 µm (2.2 µm) at the BJ to 3.0 µm (3.2 µm) at the facet region. The core thickness at the BJ was 550 nm.

The coupling loss between a fibre with a circular MFD of 3.0 µm and an SSC with a facet WG widths of 3.0 µm or 3.2 µm as a function of the facet core thickness are shown in Fig. 8. The simulations were carried out for two sets of WG widths to account for the cross wafer and wafer to wafer WG width variations. As expected the coupling loss decreases with decreasing the facet core thickness to a certain point, and then increases quickly. For smaller core thicknesses, the mode becomes leaky and the loss dramatically increases. The plot of the total loss (SSC propagation loss + coupling loss) as a function of the facet core thickness yields an optimum core thickness of 115 nm ± 10 nm. The measured total loss per facet of the fabricated SSCs are in relatively good agreement with the simulation results shown in Fig. 8. Furthermore, the calculated coupling loss for a device with no integrated SSCs is ~ 8 dB. Including the measured WG propogation loss, the total loss of a device without integrated SSCs exceeds 9 dB which is in good agreement with the data shown in Fig. 3.

Figure 9 shows the excess coupling loss as a function of input/output fibre misalignment in the lateral (paralel to the plane of the chip) and vertical (perpendicular to the plane of the chip) directions. The fibre displacement step was 0.1 µm. The 1-dB misalignment tolerance of the input fibre in the lateral (vertical) direction was 0.7 µm (0.7 µm), and the 1-dB misalignment tolerance of the output fibre in the lateral (vertical) direction was 0.8 µm (0.6 µm). These results are comparable to those reported in [9]. In an ideal case, where the input and output WGs and

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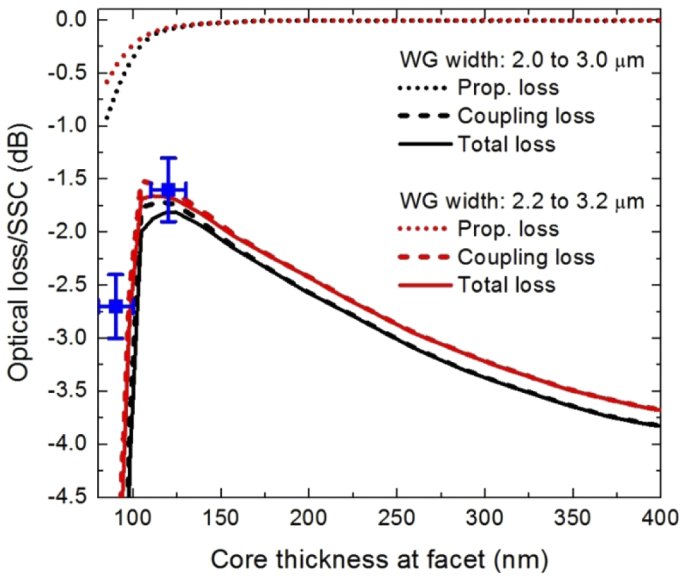

Fig. 8. Plot of the calculated SSC propagation loss, coupling loss and the total loss as a function of the facet core thickness. The fibre MFD was 3.0 μm. The core thickness at the BJ was 550 nm and the SSC taper length was 100 μm. The square data points are the experimental data in this work. Each data point represents the mean of the measurements on over 40 devices, and the vertical error bars represent one standard deviation of the measured loss values. The horizontal error bars represent one standard deviation of the core thickness variation across the wafer.

the coupling optical fibers are identical, one would expect an identical misalignment tolerance at the input and output ports. We observe ~ 0.1 dB difference at the 1dB-misalignment between the

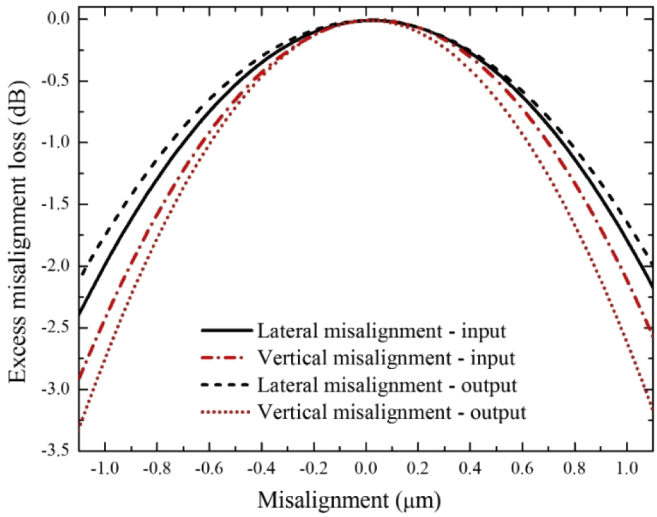

Fig. 9. Plot of the least square fits of the measured excess optical misalignment loss as a function of the input/output fibre misalignment in the lateral (parallel to the chip plane) and vertical directions (perpendicular to the chip plane).

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input and output facets. The output shows a slightly better performance in the lateral direction, while the input shows a slightly better performance in the vertical direction. These results suggest the presence of a slight asymmetry at the input/output coupling points. This is likely related to the measurement setup rather than a physical asymmetry in the input/output facets of the device. Further analysis is required to clarify the origin of this observation.

4. Conclusion

In summary, we have developed a simple fabrication method to produce a vertically tapered InGaAsP/InP WG spot size converter. This was accomplished by manipulating the lithographic system focussing plane to create a spatially varying photoresist profile that could be precisely controlled by mask feature widths. The spatially varying photoresist pattern could then be transferred to the underlying semiconductor via a dry etch process. The fibre-to-fibre loss measurements confirmed the excellent performance of the fabricated SSCs, with coupling efficiencies of 1.3 dB obtained from chip to a 3 µm MFD lensed fiber. The experimental results were consistent with the predictions from 2D FDE and 3D EME simulations.

Disclosures

The authors declare no conflicts of interest.

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